

## 7.9-11GHz 30W GaN PA MMIC

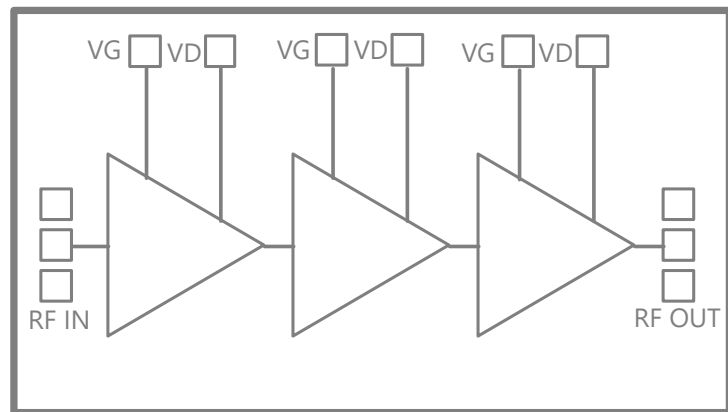
### Product Overview

ICONICRF's ICP1044P is a 3 stage MMIC power amplifier in a 6x6mm QFN package, fabricated using GaN on SiC technology. ICP1044P operates from 7.9-11GHz delivering 30W of output power, with a typical PAE of 38% across the band. ICP1044P is well suited to commercial and defence applications.

#### Key Features

- Frequency Range: 7.9-11GHz
- Pout: 44dBm Pulsed (100µs, 10%)
- PAE: 38%
- Small Signal Gain: 31dB
- Bias:  $V_{DQ}=28V$ ,  $I_{DQ}=175mA$
- Technology: GaN on SiC
- Lead-free and RoHS compliant
- Package Size: 6mm x 6mm, 40 Lead QFN
- Integrated Power Detector

#### Functional Block Diagram



#### Applications

- Commercial Radar
- Satellite Communications
- Aerospace & Defence

#### Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions <sup>(1)</sup>
Frequency	7.9		11	GHz	
Saturated Output Power, $P_{sat}$		44		dBm	$P_{in}=18dBm$
Power Added Efficiency, PAE		38		%	$P_{in}=18dBm$
Small Signal Gain, $S_{21}$		31		dB	
Input Return Loss		10		dB	
Output Return Loss		6		dB	

**Note:** (1) Test conditions unless otherwise stated  $V_{DQ}=28V$ ,  $I_{DQ}=175mA$ ,  $T_A=25^{\circ}C$ , Pulsed 100µs, 10%

## Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain Voltage ( $V_{DG}$ )	40V
Power Dissipation (CW)	TBC
CW Input Power	TBC
Channel Temperature	275°C
Storage Temperature	-65°C to +150°C

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## Note:

Exceeding any one or combination of these limits may cause permanent damage to this device.

ICONIC RF does not recommend sustained operation near these survivability limits.

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## Table of Contents

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Product Overview.....	1
1. Typical RF Performance.....	4
1.1. Typical Pulsed Power Performance.....	4
2. Pinout.....	7
3. Application Circuit.....	8
4. Mechanical Drawing.....	9
5. Evaluation Board.....	10
6. Other considerations.....	11
Microchip Information.....	12
The Microchip Website.....	12
Product Change Notification Service.....	12
Customer Support.....	12
Product Identification System.....	13
Microchip Devices Code Protection Feature.....	13
Legal Notice.....	13
Trademarks.....	14
Quality Management System.....	15
Worldwide Sales and Service.....	16

# 1. Typical RF Performance

## 1.1 Typical Pulsed Power Performance

Test conditions:  $V_{DQ}=28V$ ,  $I_{DQ}=175mA$ ,  $T_A=25^{\circ}C$  (Pulse: 100 $\mu$ s / 10%)

Figure 1-1.  $P_{OUT}$  vs Frequency

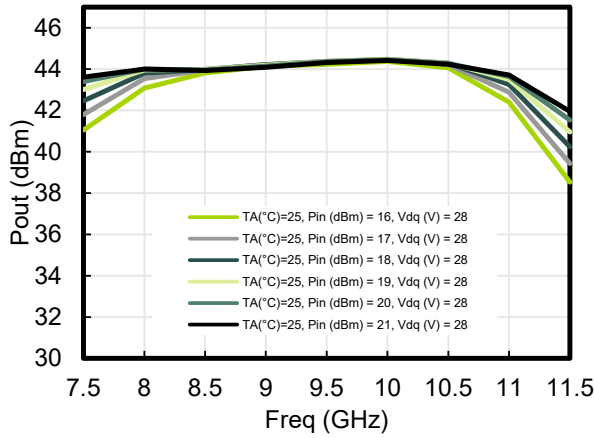


Figure 1-2. Gain vs Frequency

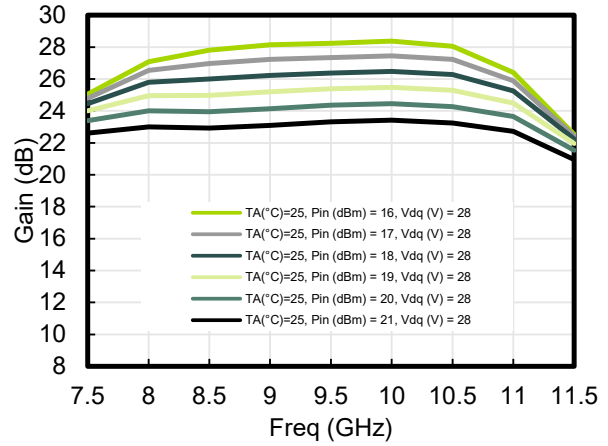


Figure 1-3. PAE vs Frequency

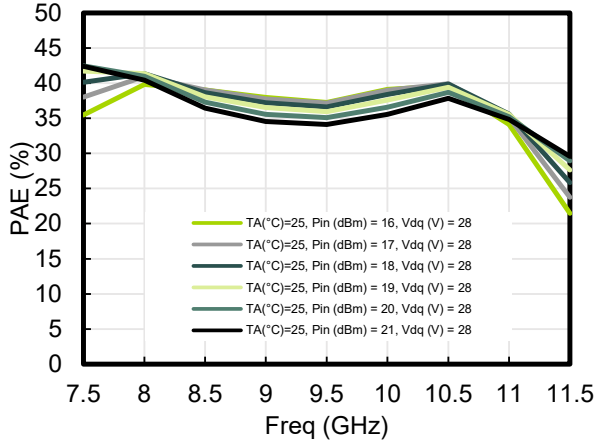
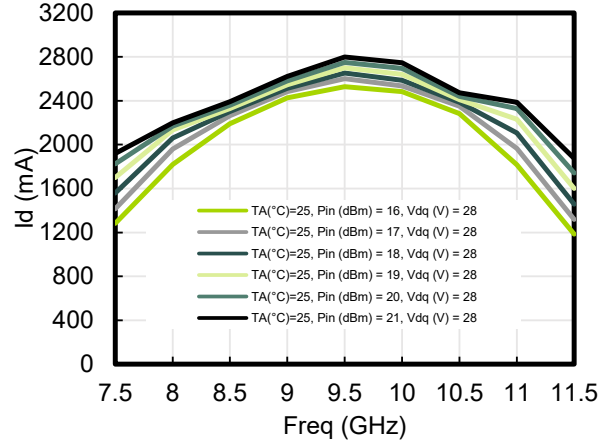


Figure 1-4.  $I_D$  vs Frequency



Test conditions:  $V_{DQ}=28V$ ,  $I_{DQ}=175mA$ ,  $T_A=25^{\circ}C$  (Pulse:  $100\mu s / 10\%$ )

Figure 1-5.  $P_{OUT}$  vs  $P_{IN}$

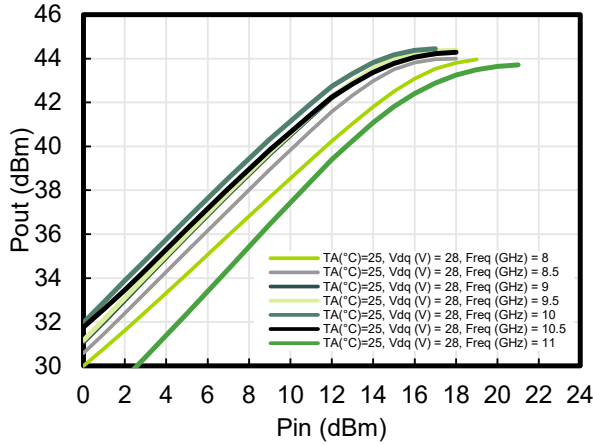


Figure 1-6. Gain vs  $P_{OUT}$

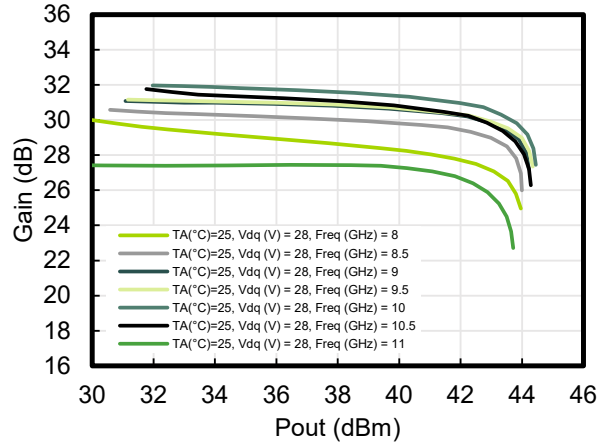


Figure 1-7. PAE vs  $P_{OUT}$

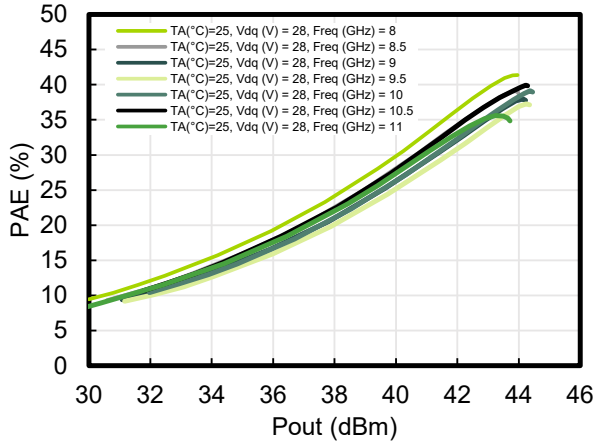


Figure 1-8.  $I_D$  vs  $P_{OUT}$

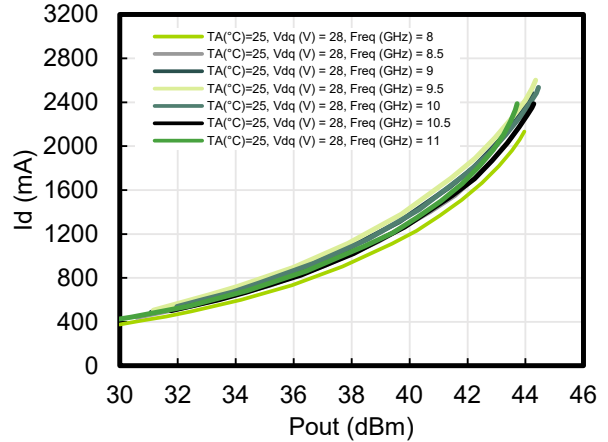
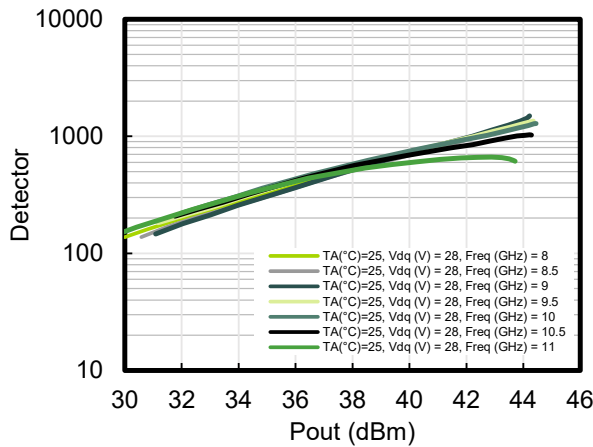


Figure 1-9. Detector vs  $P_{OUT}$



Test conditions:  $V_{DQ}=28V$ ,  $I_{DQ}=175mA$ , Freq.=9.5GHz (Pulse: 100 $\mu$ s / 10%)

Figure 1-10.  $P_{OUT}$  vs  $P_{IN}$

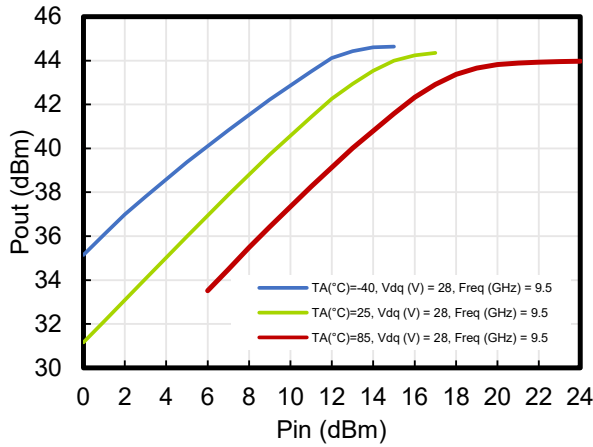


Figure 1-11. Gain vs  $P_{OUT}$

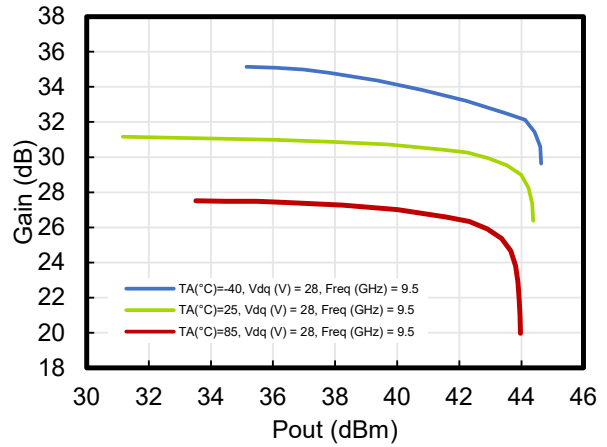


Figure 1-12. PAE vs  $P_{OUT}$

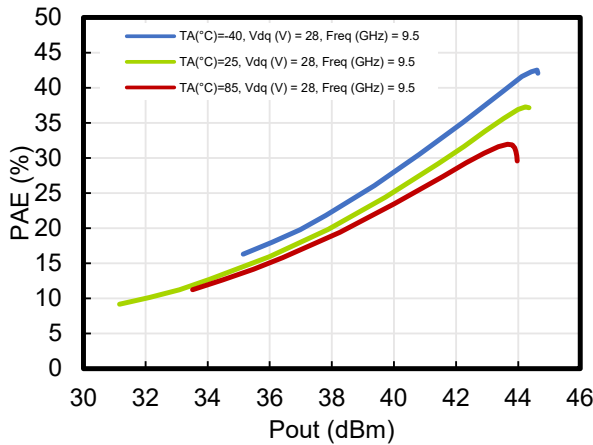
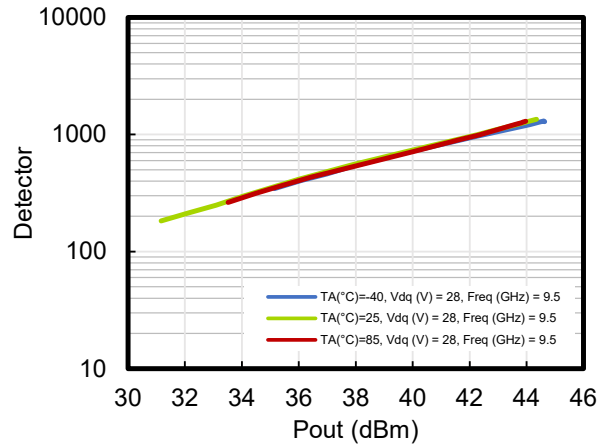


Figure 1-13. Detector vs  $P_{OUT}$



Test conditions:  $V_{DQ}=28V$ ,  $I_{DQ}=175mA$  (Pulse: 100 $\mu$ s / 10%)

Figure 1-14.  $P_{OUT}$  vs Frequency

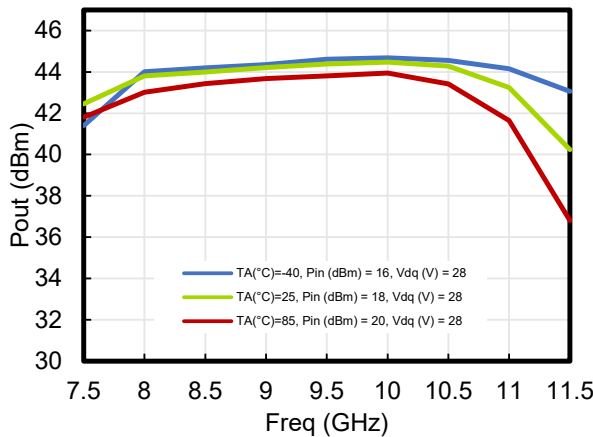
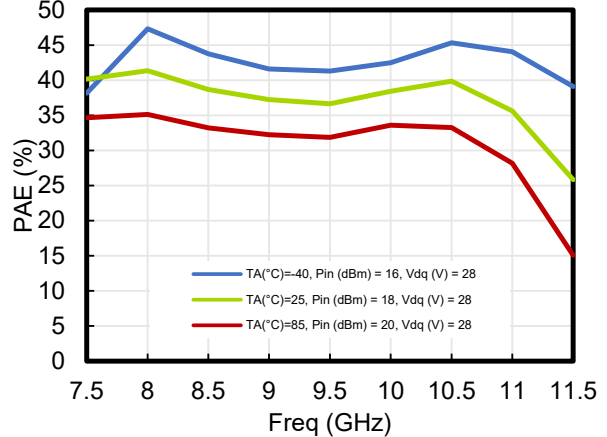
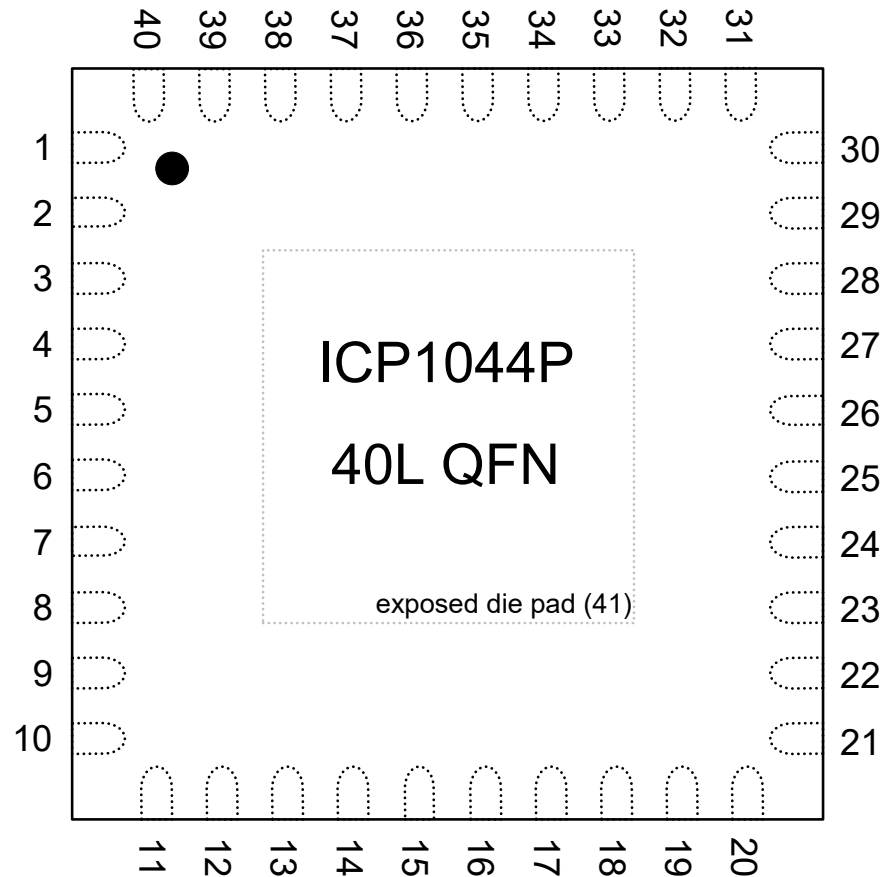


Figure 1-15. PAE vs Frequency



## 2. Pinout



Pad No.	Function	Description
1-4, 6-11, 13, 15, 18-25, 27-31, 36, 38-41	GND	Ground connection
5	RF <sub>IN</sub>	RF input, 50 ohm, DC blocked
12	V <sub>G1-2</sub> <sup>(1)</sup>	1 <sup>st</sup> and 2 <sup>nd</sup> stage gate bias, decoupling and bypass caps required
14	V <sub>G3</sub> <sup>(1)</sup>	3 <sup>rd</sup> stage gate bias, decoupling and bypass caps required
37	V <sub>D1-2</sub> <sup>(2)</sup>	1 <sup>st</sup> and 2 <sup>nd</sup> stage drain voltage, decoupling and bypass caps required
16, 17, 34, 35	V <sub>D3</sub> <sup>(2)</sup>	3 <sup>rd</sup> stage drain voltage, decoupling and bypass caps required
33	V <sub>DET</sub> <sup>(3)</sup>	Detector circuit voltage output
32	V <sub>REF</sub> <sup>(3)</sup>	Detector circuit reference voltage output
26	RF <sub>OUT</sub>	RF output, 50 ohm, DC blocked

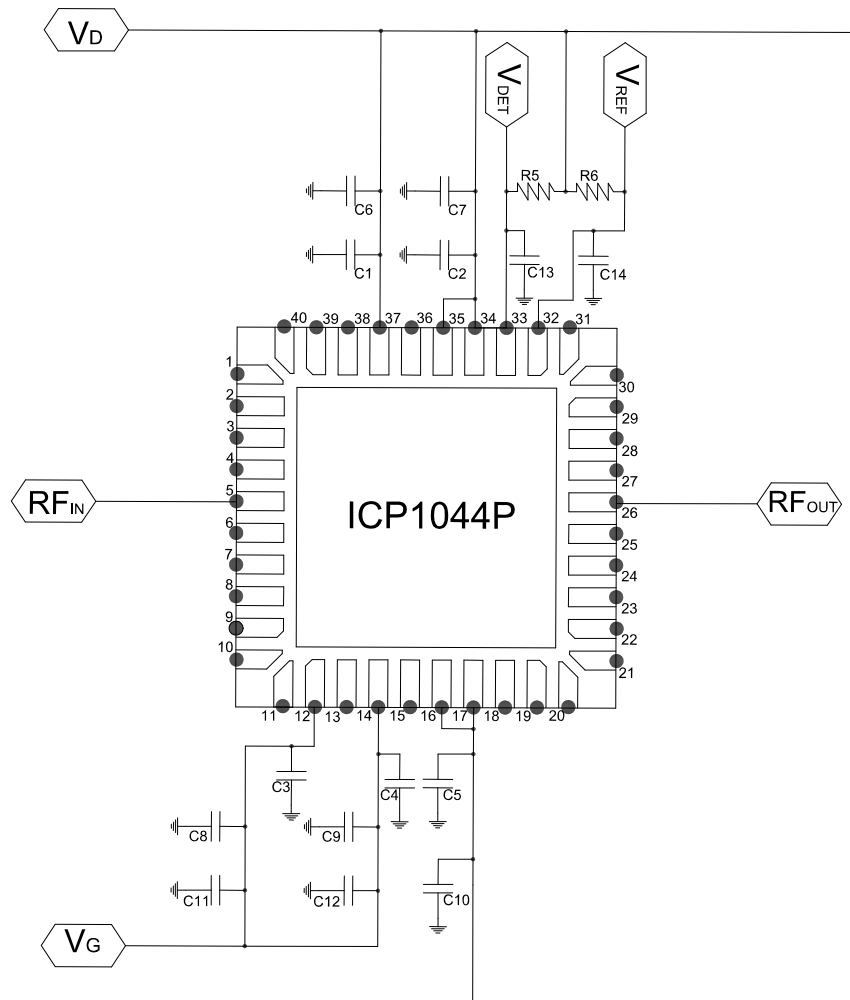
**Note:**

(1) V<sub>G1-2</sub> and V<sub>G3</sub> can be connected together in application.

(2) V<sub>D1-2</sub> and V<sub>D3</sub> can be connected together in application.

(3) Applications requiring power detector may use pins 32 and 33, otherwise pins should be NC or Ground

### 3. Application Circuit

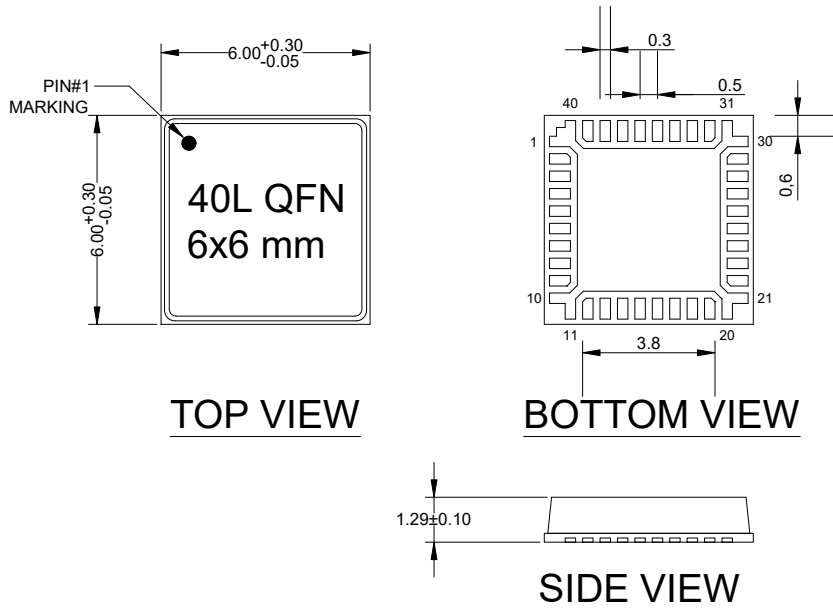


Component ID	Value	Details	Qty	Manufacturer Part No.
C1-C5, C13 <sup>(1)</sup> , C14 <sup>(1)</sup>	1000pF	1000pF CAP 0402, C0G, 50V	9	Various
C6-C10	10nF	10nF CAP 0603, C0G, 50V	5	Various
C11, C12	1μF	1μF CAP 0805, C0G, 50V	2	Various
R5 <sup>(1)</sup> , R6 <sup>(1)</sup>	100kΩ	100kΩ RES 0402	4	Various

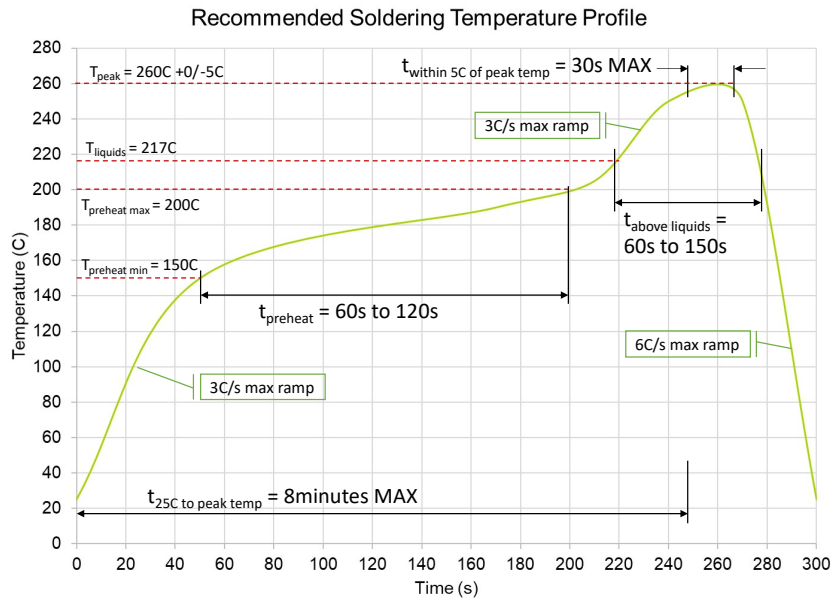
**Note:** (1) Applications requiring power detector may use either pin numbers 33 and 32. Otherwise pins 33 and 32 should be NC or ground and components R5, R6, C13 & C14 are not required



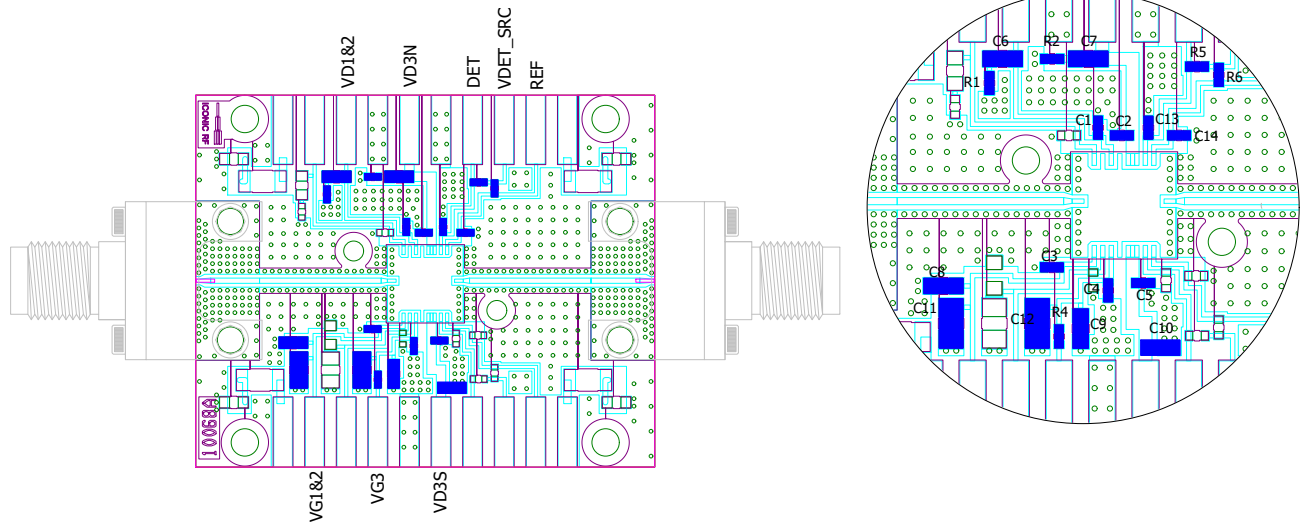
4. Mechanical Drawing



Units: mm



## 5. Evaluation Board



### Evaluation board construction

- Board Size: 37mm x 30mm 4 layer PCB:
  - 1oz Cu, Au finish RO4003C 10mil
  - 0.5oz Cu 370HR 6mil
  - 0.5oz Cu 370HR 6mil
  - 1oz Cu, Au finish
  - Solid Copper Coin over plated
  - Via size: 0.3mm plated
- Baseplate: Solid copper 37mm x 50mm x 10mm, Au plated

Component ID	Value	Details	Qty	Manufacturer Part No.
C1-C5, C13 <sup>(1)</sup> , C14 <sup>(1)</sup>	1000pF	1000pF CAP 0402, C0G, 50V	7	Various
C6-C10	10nF	10nF CAP 0603, C0G, 50V	5	Various
C11, C12	1μF	1μF CAP 0805, C0G, 50V	2	Various
R1-R4	0Ω	0Ω RES 0402	4	Various
R5 <sup>(1)</sup> , R6 <sup>(1)</sup>	100kΩ	100kΩ RES 0402	2	Various

**Note:** (1) These components are used for the detector circuit on package pins 33 and 32. This circuit is optional and the components can be omitted if the circuit is not required

## 6. Other considerations

### **Bias-up procedure**

1. Set  $V_G$  to -5V
2. Set  $V_D$  to 28V
3. Adjust  $V_G$  positive until  $I_D$  quiescent is 175mA
4. Limit  $I_D$  to 3A
5. Apply RF signal

### **Bias-down procedure**

1. Turn off RF
2. Turn off  $V_D$ , allow drain capacitors to discharge
3. Turn off  $V_G$

### **Solderability**

Compatible with the latest version of J-STD-020 Lead free solder.

### **Handling procedures**

Please observe the following precautions to avoid damage:

### **Static Sensitivity**

Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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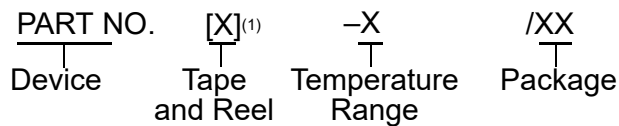
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	T	= Tape and Reel <sup>(1)</sup>
Temperature Range:	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Extended)
Package: <sup>(2)</sup>	JQ	= UQFN
	P	= PDIP
	ST	= TSSOP
	SL	= SOIC-14
	SN	= SOIC-8
	RF	= UDFN
Pattern:	QTP, SQTP <sup>SM</sup> (Serial Quick Turn Programming capability), Code or Special Requirements (blank otherwise)	

- Device A - I/P Industrial temperature, PDIP package
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PIS\_NOTES

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