

## Product Overview

ICP1240 is a 3 stage MMIC power amplifier in bare die form, fabricated using GaN on SiC technology. ICP1240 operates from 6-18GHz with 41dBm output power, >20% PAE and 23dB typical small signal gain. ICP1240 is well suited to a variety of commercial, aerospace and defense applications.

### Key Features

- **Frequency Range: 6-18GHz**
- **P<sub>out</sub>: 41dBm @P<sub>in</sub>=24dBm**
- **PAE: 20% @P<sub>in</sub>=24dBm**
- **Small Signal Gain: 23dB**
- **Bias: V<sub>D</sub>=24V, I<sub>DQ</sub>=280mA**
- **Technology: GaN on SiC**
- **Lead-free and RoHS compliant**
- **CW operation**
- **Die Size: 5.01mm x 3.3mm**

### Applications

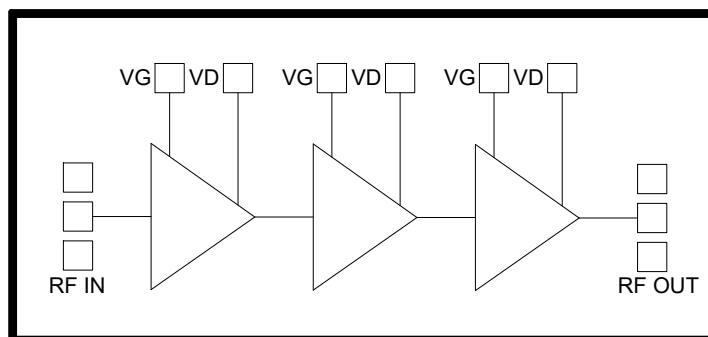
- Test and Measurement
- Aerospace & Defense

### Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions <sup>(1)</sup>
Frequency	6		18	GHz	
Output Power @P <sub>sat</sub>	40	41		dBm	P <sub>in</sub> =24dBm
Gain @P <sub>sat</sub>	17	18.5	20		P <sub>in</sub> =24dBm
Power Added Efficiency, PAE @P <sub>sat</sub>		20		%	P <sub>in</sub> =24dBm
Drain current (I <sub>d</sub> ) @P <sub>sat</sub>	2200		3850	mA	P <sub>in</sub> =24dBm
Gate voltage (V <sub>G</sub> ) for I <sub>DQ</sub>	-1.7		-2.2	V	
Gate current (I <sub>g</sub> )	-2		10	mA	P <sub>in</sub> =24dBm
Small Signal Gain, S <sub>21</sub>		23		dB	
Input Return Loss		15		dB	
Output Return Loss		7		dB	
Recommended operating voltage	18	24	24	V	

**Note:** (1) Test conditions unless otherwise stated V<sub>D</sub>=24V, I<sub>DQ</sub>=280mA, T<sub>A</sub>=25°C, CW

### Functional Block Diagram



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# 1. Electrical Specification

## 1.1 Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain Voltage ( $V_D$ )	30V
CW Drain Current ( $I_D$ ), $T_A=25^\circ\text{C}$	6A
Gate Voltage Range ( $V_G$ )	-5 to 0V
Gate Current ( $I_G$ )	14mA
Power Dissipation (CW) $T_A=25^\circ\text{C}$	140W
Power Dissipation (CW) $T_A=85^\circ\text{C}$	110W
CW Input Power 50Ohm, $T_A=25^\circ\text{C}$	+29dBm
Input Power VSWR (2:1) $V_D=20\text{V}$ , $I_{DQ}=280\text{mA}$ $V_D=24\text{V}$ , $I_{DQ}=280\text{mA}$	+27dBm
Channel Temperature	275°C
Storage Temperature	-65°C to +150°C
Eutectic Die Attached Temperature (30s)	320°C

### Thermal and Reliability

Parameter	Value
Thermal Resistance	1.71°C/W

- Assumes silver sintered epoxy attach (15µm thick) mounted on CuMo carrier.
- Base temperature is assumed at the top of the CuMo carrier
- Thermal resistance calculated using IR measurement of the channel temperature.

**Note:**

Exceeding any one or combination of these limits may cause permanent damage to this device.

Microchip Technology Inc. does not recommend sustained operation near these survivability limits.

## 1.2 Small Signal Performance

### Typical Data over $V_D$

Test conditions:  $I_{DQ}=280\text{mA}$ ,  $T_A=25^\circ\text{C}$

Figure 1-1.  $S_{21}$  vs Freq

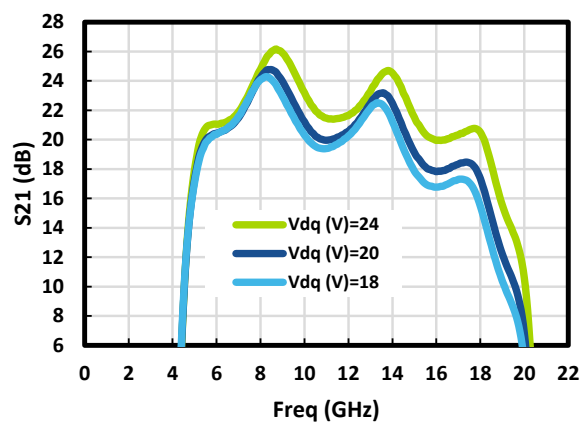


Figure 1-2.  $S_{11}$  vs Freq

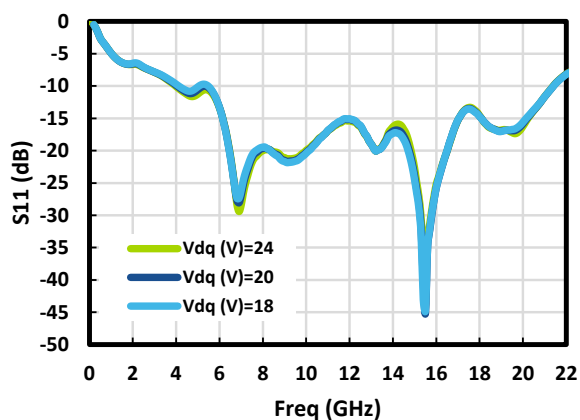
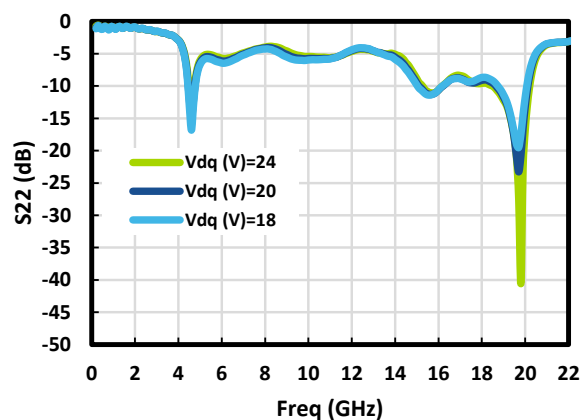
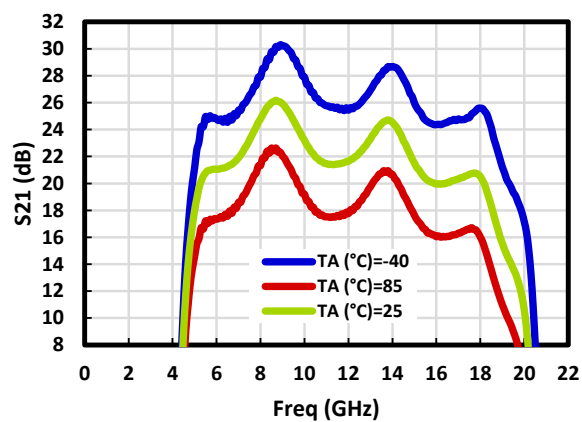
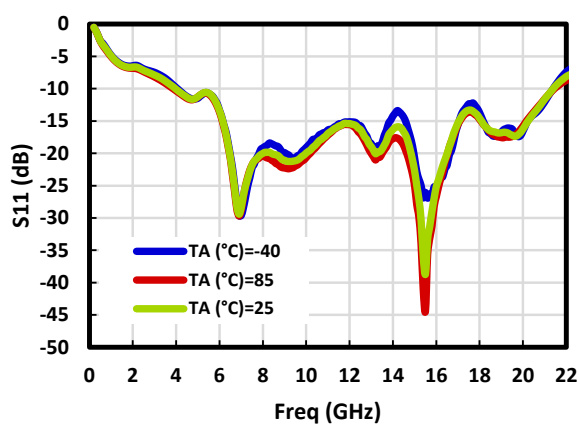
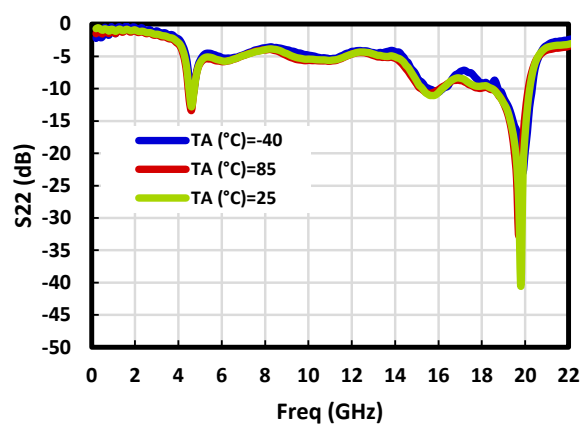


Figure 1-3.  $S_{22}$  vs Freq



**Typical Data over T<sub>A</sub>**Test conditions: V<sub>D</sub>=24V, I<sub>DQ</sub>=280mA**Figure 1-4.** S<sub>21</sub> vs Freq**Figure 1-5.** S<sub>11</sub> vs Freq**Figure 1-6.** S<sub>22</sub> vs Freq

### 1.3 Large Signal Performance

#### Typical CW Power Data

Test conditions:  $V_D=24V$ ,  $I_{DQ}=280mA$ ,  $T_A=25^\circ C$ , CW

Figure 1-7.  $P_{out}$  vs.  $P_{in}$

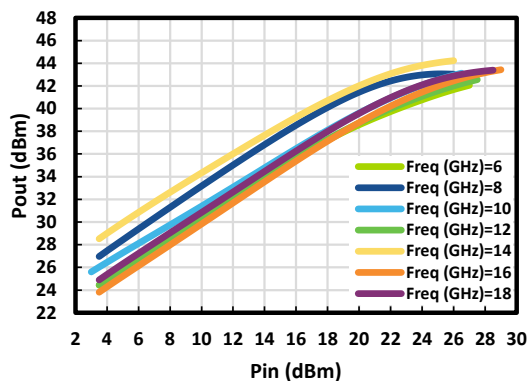


Figure 1-8. Gain vs.  $P_{out}$

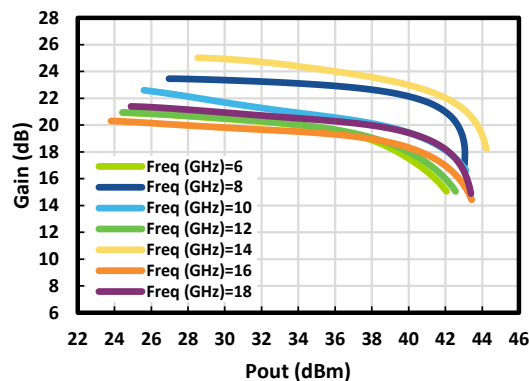


Figure 1-9. PAE vs.  $P_{out}$

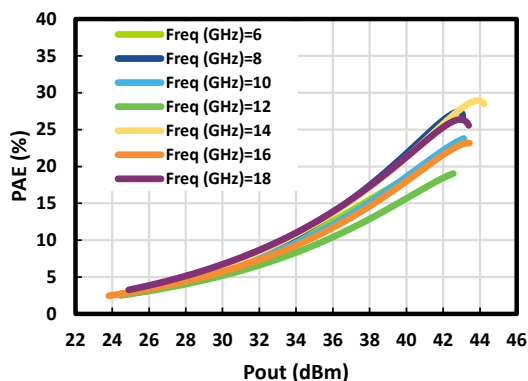


Figure 1-10.  $I_D$  vs.  $P_{out}$

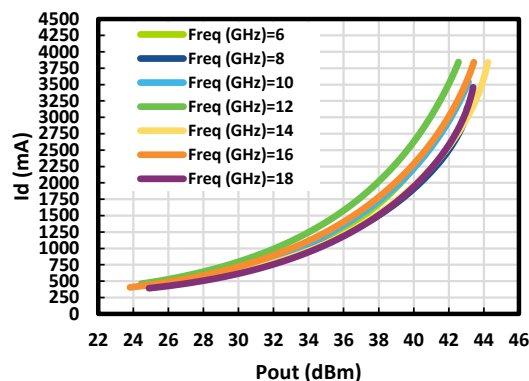


Figure 1-11.  $P_{out}$  vs. Freq.

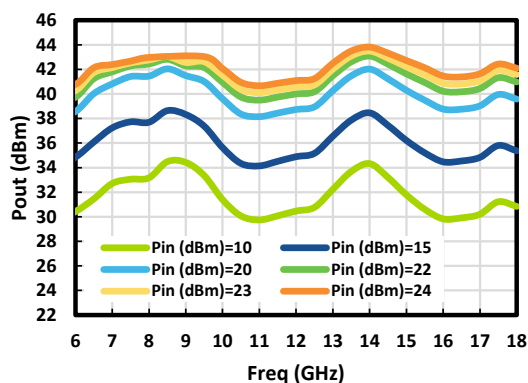
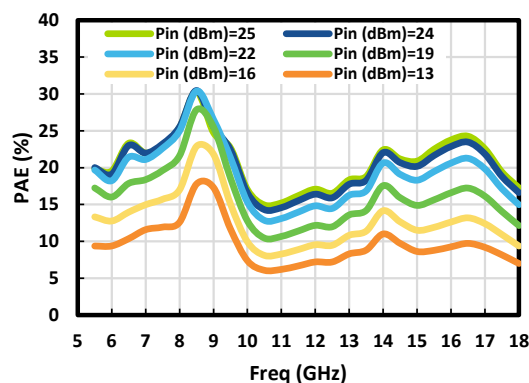


Figure 1-12. PAE vs. Freq.



### Typical CW Power Data over $V_D$

Test conditions:  $I_{DQ}=280\text{mA}$ ,  $T_A=25^\circ\text{C}$ , CW

Figure 1-13. Gain vs.  $P_{in}$  at 6GHz

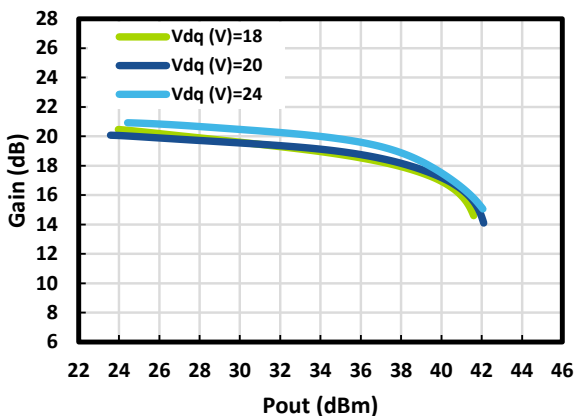


Figure 1-14. Gain vs.  $P_{out}$  at 10GHz

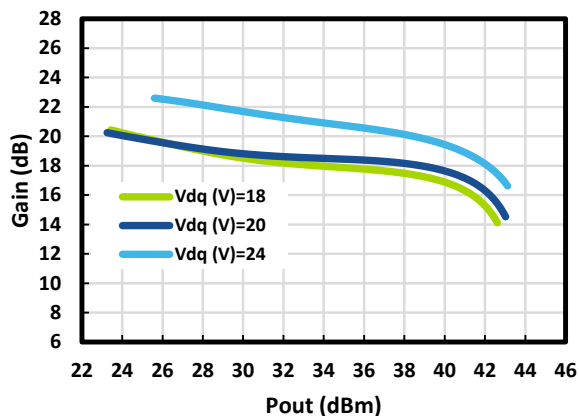


Figure 1-15. Gain vs.  $P_{in}$  at 14GHz

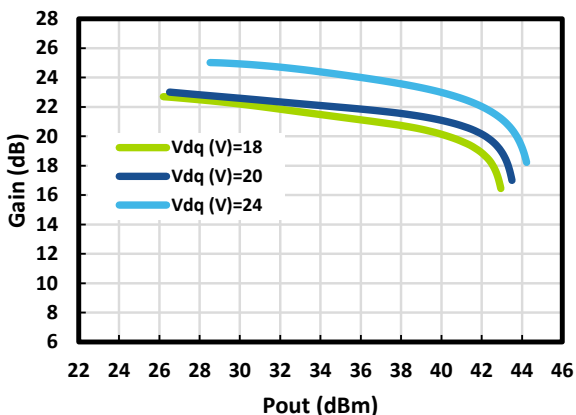


Figure 1-16. Gain vs.  $P_{out}$  at 18GHz

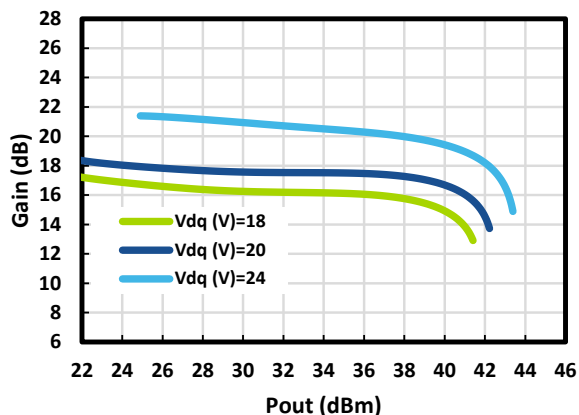


Figure 1-17.  $P_{out}$  vs. Freq.

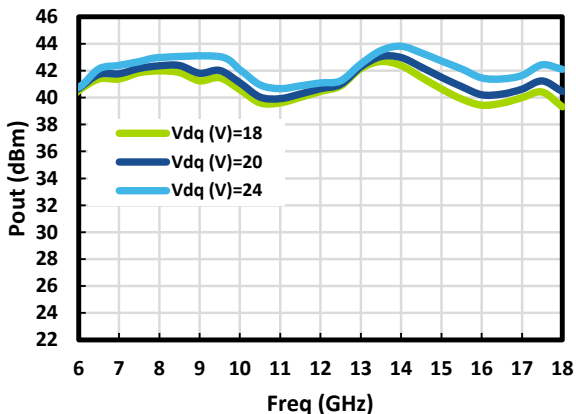
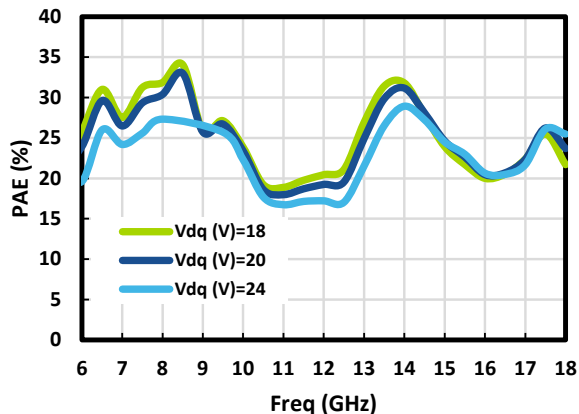


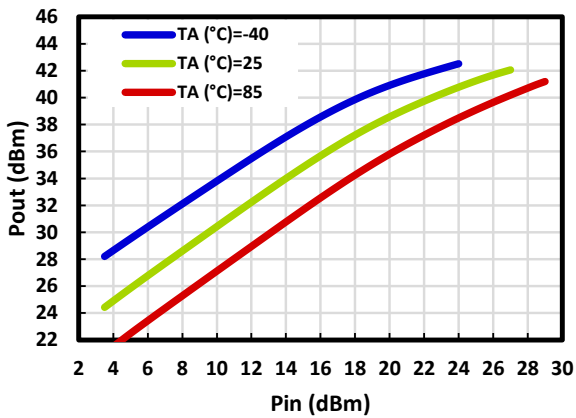
Figure 1-18. PAE vs. Freq.



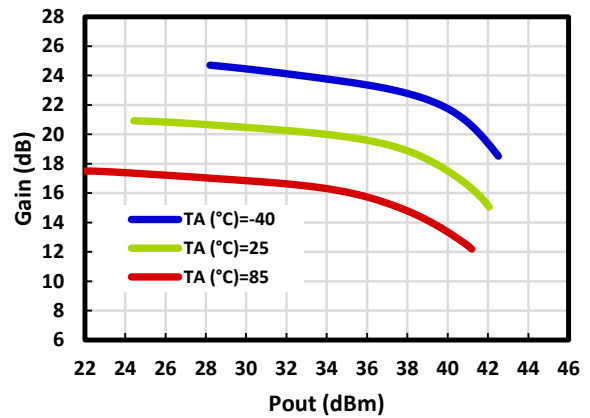
**Typical CW Power Data over  $T_A$**

Test conditions:  $V_D=24V$ ,  $I_{DQ}=280mA$ , CW

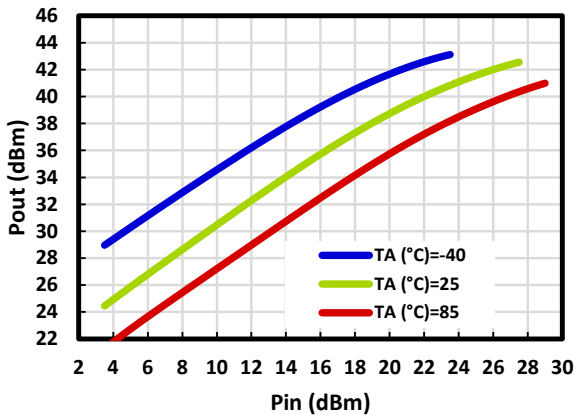
**Figure 1-19.**  $P_{out}$  vs.  $P_{in}$  at 6GHz



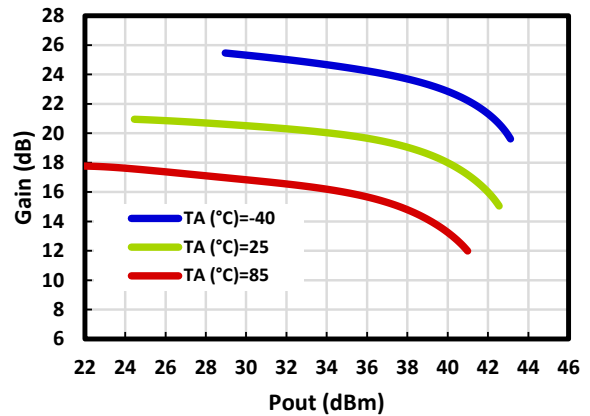
**Figure 1-20.** Gain vs.  $P_{out}$  at 6GHz



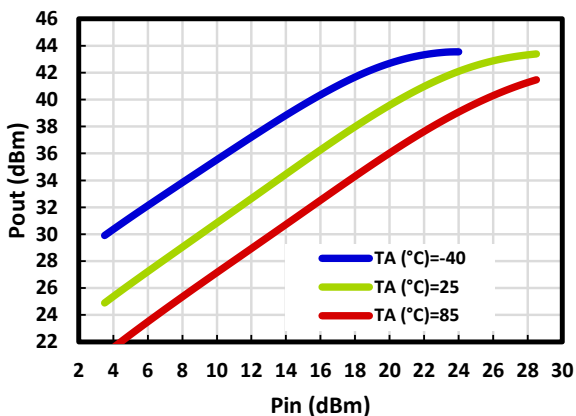
**Figure 1-21.**  $P_{out}$  vs.  $P_{in}$  at 12GHz



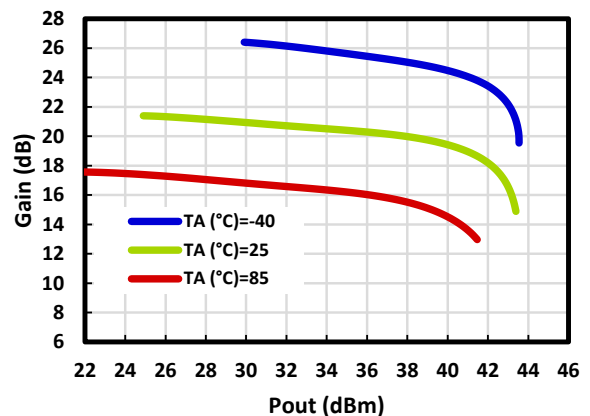
**Figure 1-22.** Gain vs.  $P_{out}$  at 12GHz



**Figure 1-23.**  $P_{out}$  vs.  $P_{in}$  at 18GHz



**Figure 1-24.** Gain vs.  $P_{out}$  at 18GHz





## Typical CW Power Data over $T_A$ (Continued)

Test conditions:  $V_D=24V$ ,  $I_{DQ}=280mA$ , CW

Figure 1-25. PAE vs.  $P_{out}$  at 6GHz

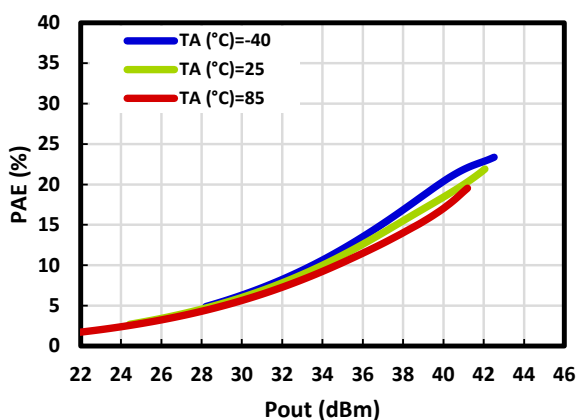


Figure 1-26.  $I_d$  vs.  $P_{out}$  at 6GHz

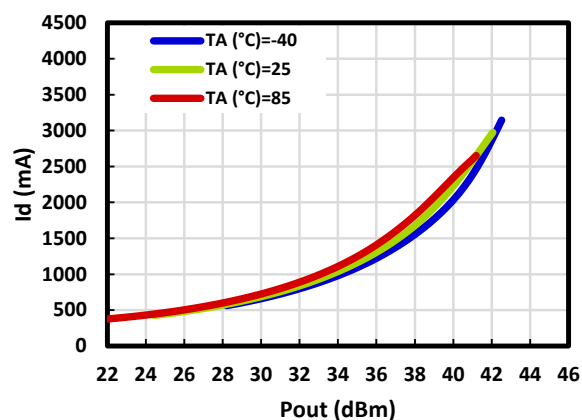


Figure 1-27. PAE vs.  $P_{out}$  at 12GHz

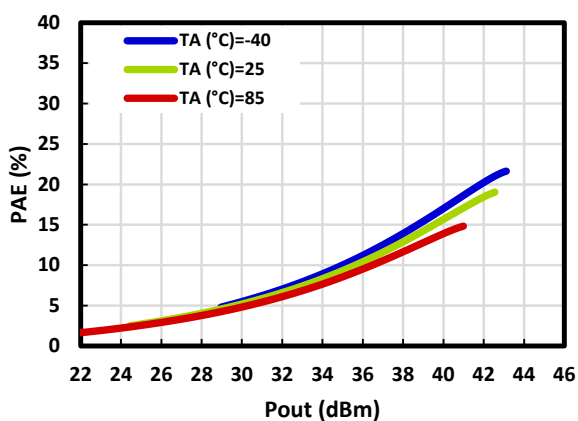


Figure 1-28.  $I_d$  vs.  $P_{out}$  at 12GHz

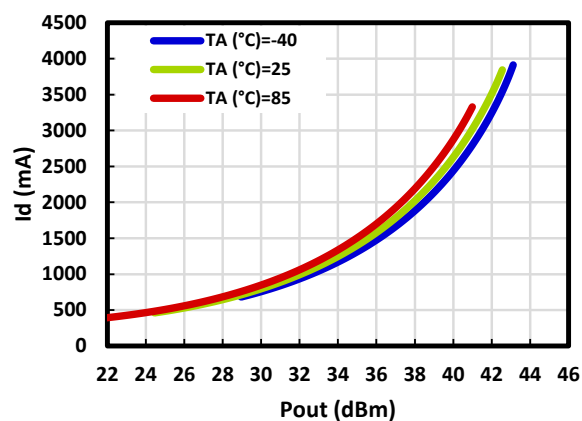


Figure 1-29. PAE vs.  $P_{out}$  at 18GHz

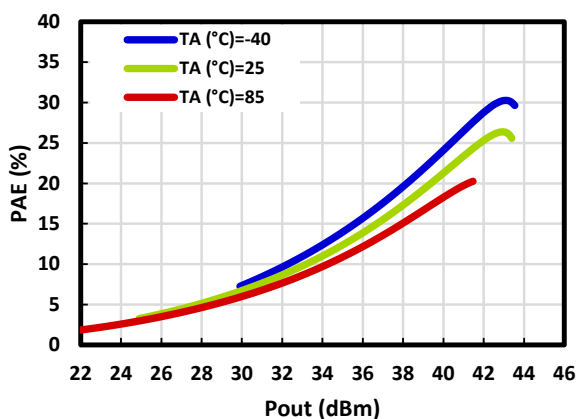
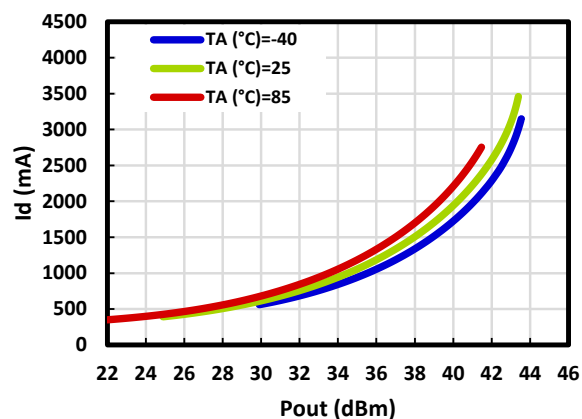


Figure 1-30.  $I_d$  vs.  $P_{out}$  at 18GHz



### Typical CW Power Data over T<sub>A</sub> (Continued)

Test conditions: V<sub>D</sub>=24V, I<sub>DQ</sub>=280mA, CW

Figure 1-31. P<sub>out</sub> vs. Freq.

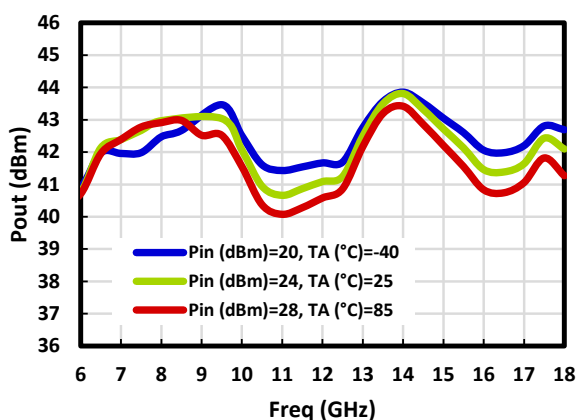
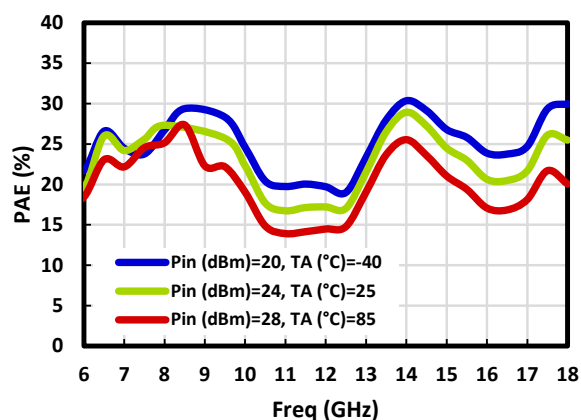


Figure 1-32. Gain vs. Freq.



### Typical CW Linearity Power Data

Test conditions: V<sub>D</sub>=24V, I<sub>DQ</sub>=280mA, T<sub>A</sub>=25°C, CW

Figure 1-33. IM<sub>3</sub> vs. P<sub>out</sub>

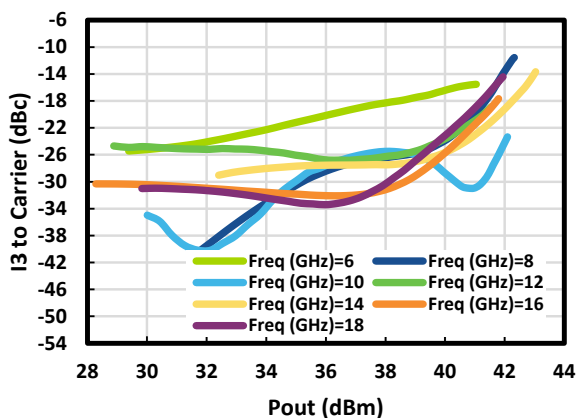
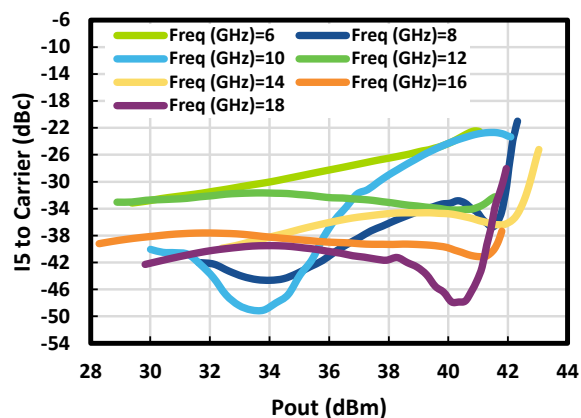
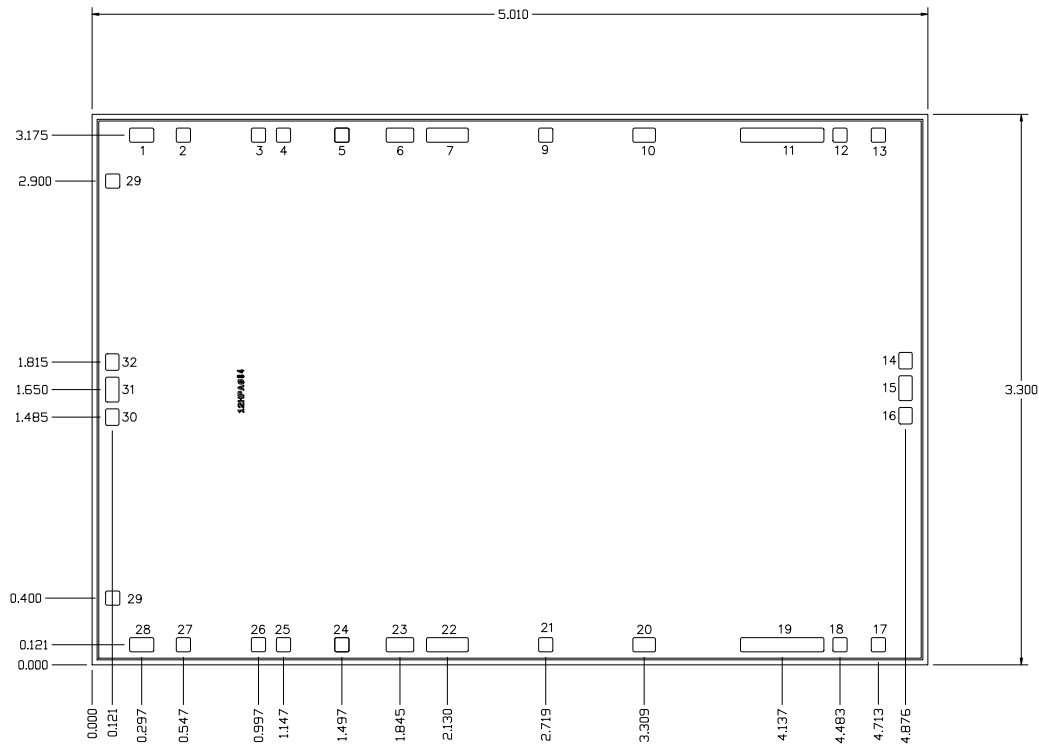


Figure 1-34. IM<sub>5</sub> vs. P<sub>out</sub>



## 2. Mechanical Drawing

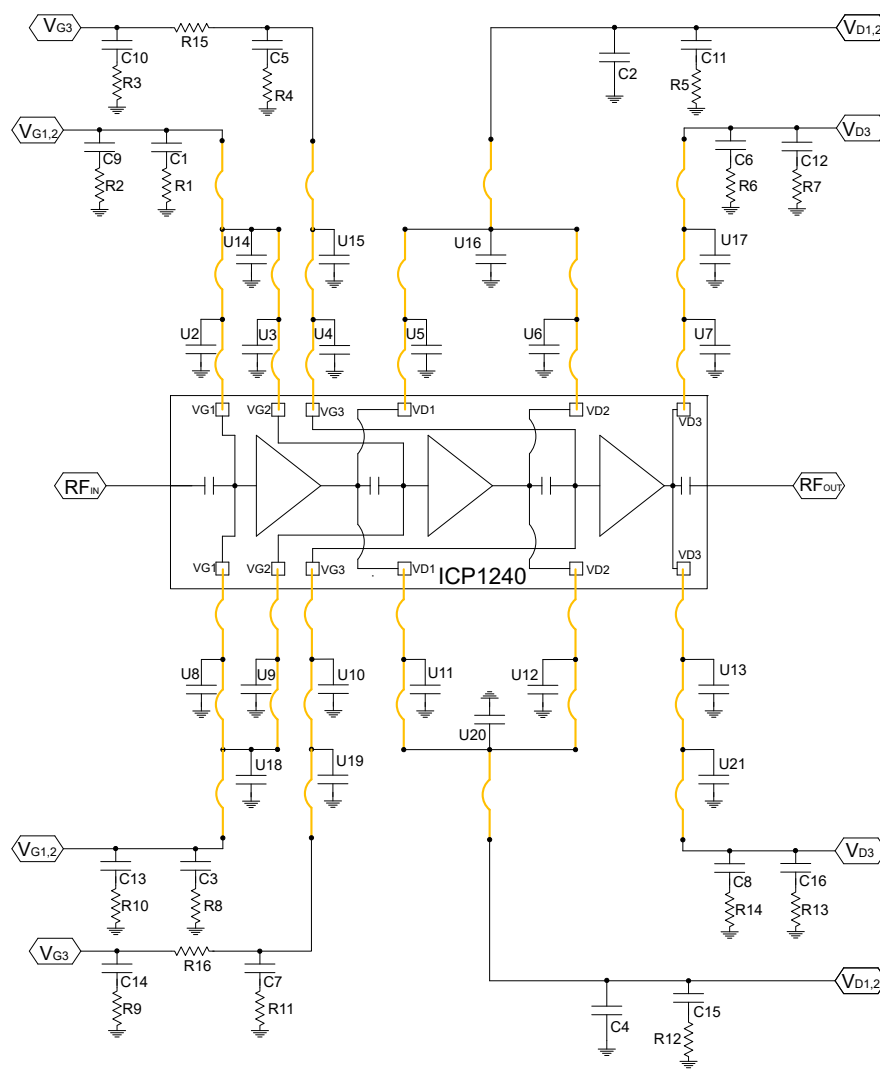


Units: mm | Thickness: 100 $\mu$ m | Backside of Die is RF and DC ground

Pad No.	Pad Dimension ( $\mu$ m)	Function	Description
1, 10, 20, 28	145x85	GND	Ground connection
3, 12, 13, 17, 18, 26	85x85	GND	Ground connection
2, 27	85x85	V <sub>G1</sub>	First stage north gate bias, decoupling and bypass caps required, must be biased from both sides
4, 25	85x85	V <sub>G2</sub>	Second stage gate bias, decoupling and bypass caps required, must be biased from both sides
5, 24	85x85	V <sub>G3</sub>	Third stage gate bias, decoupling and bypass caps required, must be biased from both sides
9, 24	85x85	No Connect	Do not connect
6, 23	165x85	V <sub>D1</sub>	First stage north drain voltage, decoupling and bypass caps required, must be biased from both sides
7, 22	250x85	V <sub>D2</sub>	Second stage drain voltage, decoupling and bypass caps required, must be biased from both sides
11, 19	500x85	V <sub>D3</sub>	Third stage drain voltage, decoupling and bypass caps required, must be biased from both sides
14, 16, 30, 32	85x100	GND	Ground connection
15	80x150	RF <sub>out</sub>	50 ohm RF output, DC blocked, pad is DC grounded
31	80x150	RF <sub>in</sub>	50 ohm RF input, DC blocked

1. V<sub>D1</sub>, V<sub>D2</sub> and V<sub>D3</sub> can be connected together in application
2. V<sub>G1</sub>, V<sub>G2</sub> and V<sub>G3</sub> can be connected together in application

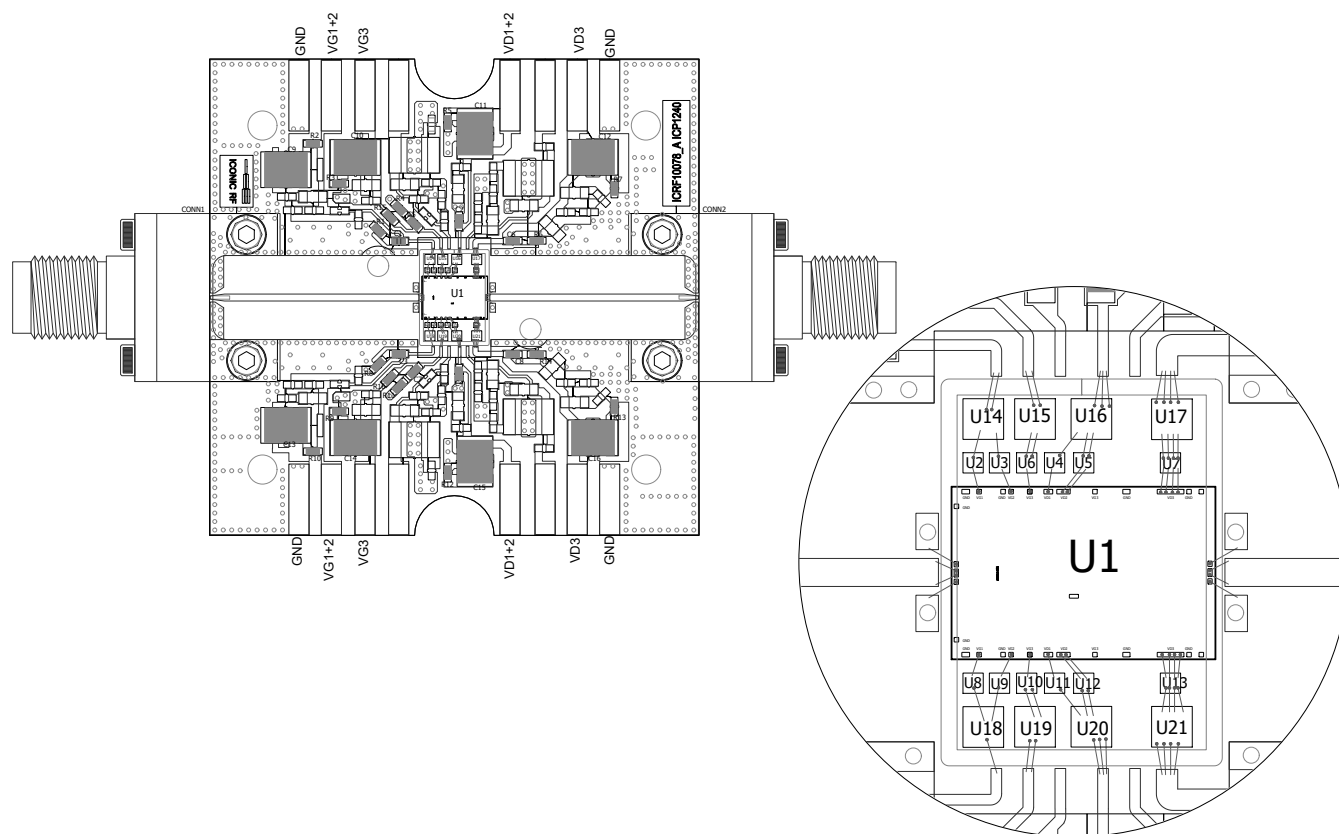
### 3. Application Circuit



#### Bill of materials

Component ID	Value	Details	Qty	Manufacturer Part No.
U2-U13	100pF	100pF SLC	12	Johanson Dielectrics Inc.
U14 - U21	10nF	10nF SLC	8	Johanson Dielectrics Inc.
C1, C3, C5, C7	100nF	100nF Capacitor,10%,50V,0402	4	Various
C2, C4, C6, C8	10nF	10nF Capacitor,10%,50V,0402	4	
C9-C16	10μF	10μF Capacitor,10%,50V,1206	8	Various
R1-R5, R7-R13	5.1Ω	5.1 ohm resistor, 0402	12	Various
R6, R14	0Ω	0 Ohms Resistor,0402	2	Various
R15, R16	82Ω	82 Ohms Resistor,0402	2	

## 4. Evaluation Board



### Die Attach Methods

PCB Construction	Material	Dimensions
METAL_1_TOP	Cu + ENIG	1oz Copper plated Electroless Nickel 3-5µm Immersion Gold 0.5µm
DIELECTRIC	RO4350C	10mils (254µm)
METAL2_BOTTOM	Cu + ENIG	1oz Copper plated Electroless Nickel 3-5µm Immersion Gold 0.5µm

Key Features	Dimensions
VIA Drill	0.3mm
VIA Plating Thickness	50-70µm
50Ohm LINE WIDTH	525µm

## 5. Other considerations

### Assembly Guidance

Interconnect assembly Notes	Die attach using Eutectic
<ul style="list-style-type: none"> <li>· Ball Bonding is preferred technique</li> <li>· Force, time and ultrasonic parameters are critical.</li> <li>· Aluminum wire bonding is not recommended.</li> <li>· Bond Wire diameter of 1mil is recommended.</li> </ul>	<ul style="list-style-type: none"> <li>· Flux-less gold-tin (AuSn) (80% Au, 20% Sn with a melting point of 280°C) preform is preferred between the die and attached surface.</li> <li>· Recommended preform should be approximately 0.0012" thick.</li> <li>· Die bonder using heated collet with a temperature of 310°C and die scrubbing should be used to ensure wetting and prevent formation of voids.</li> <li>· Exposure to extreme temperature should be kept to a minimum.</li> <li>· The optimum die attach environment is nitrogen atmosphere.</li> </ul>
Die attach of component using adhesive	Re-flow Process
<ul style="list-style-type: none"> <li>· Vacuum collets are preferred method of pickup.</li> <li>· Pickup method must consider the avoidance of die air bridges.</li> <li>· Die suitable for Eutectic and Epoxy die attach.</li> <li>· Where Epoxy is used, high thermal conductivity Silver Sintered Epoxy is recommended:-</li> <li>· Kyocera CT2700R7S</li> <li>· Namics H9889-1</li> </ul>	<ul style="list-style-type: none"> <li>· Maximum temperature 320°C for 30 seconds.</li> <li>· Material matching for coefficient of thermal expansion is crucial for long-term reliability</li> </ul>

Optimum RF power performance achieved by minimizing output RF bond wire length.

For optimum RF and thermal performance IconicRF recommends the die assembly base plate is adequately bolted to an forced air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 170 $\mu$ m thick) for optimal heat transfer. There are many variables of the second level assembly between the die base plate and heat sink that IconicRF are unable to control and the following guidance is provided as information only. Fixing bolts should be provided as close to the die as possible to ensure an optimum pressure between the base plate and the heat sink. The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised all surfaces be cleaned and be free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star shaped pattern to a recommended torque of 2.5N/m.

#### Bias-up procedure

1. Set  $V_G$  to -5V
2. Set  $V_D$  to 20V-24V
3. Adjust  $V_G$  positive until  $I_D$  quiescent is 280mA
4. Limit  $I_D$  to 4.5A
5. Apply RF signal

#### Bias-down procedure

1. Turn off RF
2. Turn off  $V_D$ , allow drain capacitors to discharge
3. Turn off  $V_G$

## 6. Ordering, Shipping, and Handling

### Handling Recommendations

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

### Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Description
ICP1240-1-110I	Bare Die in Gelpak
EV29N87A	Evaluation Board Development Tool for ICP1240-1-110I

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
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