ICONIC RF

a MICROCHIP company

6-18GHz 10W GaN PA MMIC

ICP1240P

Product Overview

ICONICRF's ICP1240P is a 3 stage MMIC power amplifier in package form, fabricated using GaN on SiC technology. ICP1240P operates from 6-18GHz with 40 dBm output power, >20% PAE and 23dB typical small signal gain. ICP1240P is well suited to a variety of commercial, aerospace and defense applications.

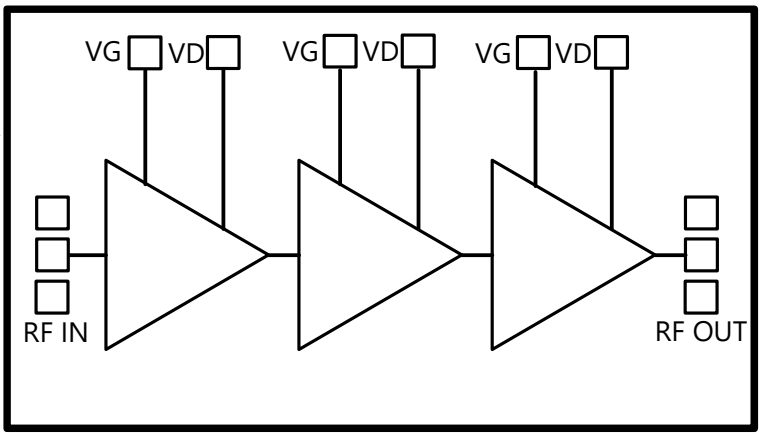
Key Features

- Frequency Range: 6-18GHz
- Pout: 40 dBm @ 24dBm Pin
- Typical PAE: 20 %
- Small Signal Gain: 23dB
- Bias: V_D=24V I_{DQ}=280mA, Typical Vg=-1.8V
- Technology: GaN on SiC
- Lead-free and RoHS compliant
- Package Dimensions 10mm x 20mm

Applications

- Test and Measurement
- Aerospace & Defense

Functional Block Diagram



Electrical Specifications | Test Conditions unless otherwise stated | V_D=*24V,* I_D=*280mA, TA*=25 °C, CW

Parameter	Conditions	Min	Typ	Max	Units
Frequency		6		18	GHz
Output Power @ P_{sat}	Pin=24dBm		40		dBm
PAE @ P_{sat}	Pin=24dBm		22		%
Small Signal Gain			23		dB
Input Return Loss			15		dB
Output Return Loss			7		dB

Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain Voltage (V_D)	30.0V
Gate Voltage Range (V_G)	-5 to 0V
Gate Current (IG)	14mA
Drain Current (CW) T_A=25ºC	5.9A
Power Dissipation (CW) T_A=25ºC Power Dissipation (CW) T_A=85ºC	140W 108W
CW Input Power 50ohm, T_A=25ºC	+29dBm
Channel Temperature	275°C
Storage Temperature	-65°C to +150°C
Input Power VSWR (2:1), V_D=20V, I_{DQ}=280mA V_D=24V, I_{DQ}=280mA	27dBm
Eutectic Die Attach Temperature (30s)	320°C

Exceeding any one or combination of these limits may cause permanent damage to this device.
ICONIC RF does not recommend sustained operation near these survivability limits.

Thermal and Reliability

Parameter	Value
Thermal Resistance	1.75ºC/W

Notes

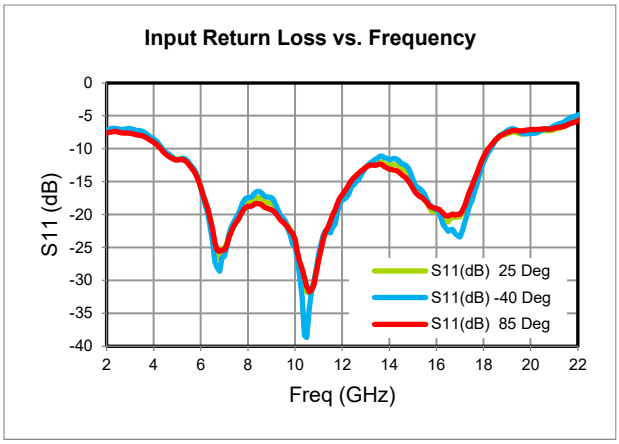
1. Assumes silver sintered epoxy attach (15um thick) mounted on CuMo carrier.
2. Base temperature is assumed at the top of the CuMo carrier
3. Thermal resistance calculated using IR measurement of the channel temperature.

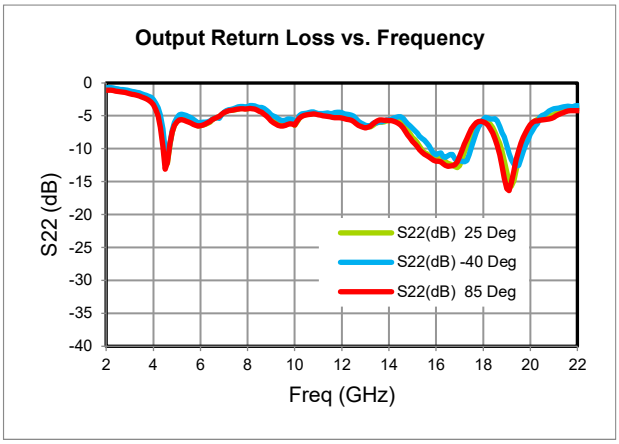
Ordering Information

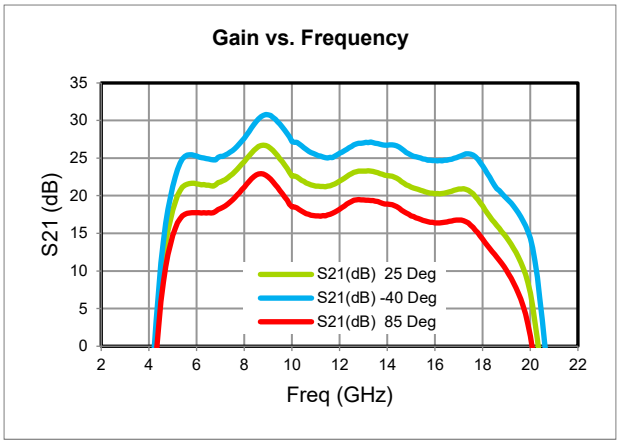
Part No.	Description
ICP1240-1-451I	Ceramic Flange Package
ICP1240-2-501U	Evaluation Board with SMA connectors

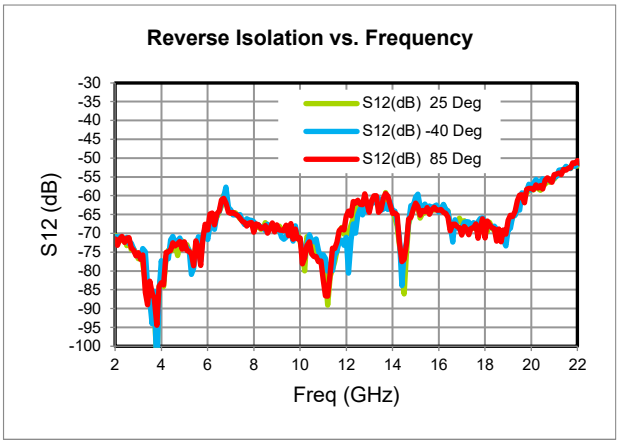
Typical Performance

Typical Small Signal Data | Test conditions unless otherwise stated V_D=24V, I_{DQ}=280mA ,TA=25 °C, CW



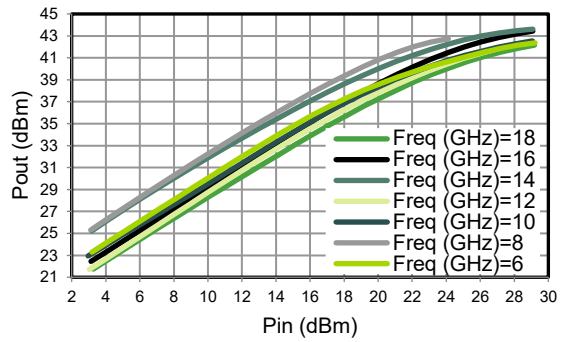




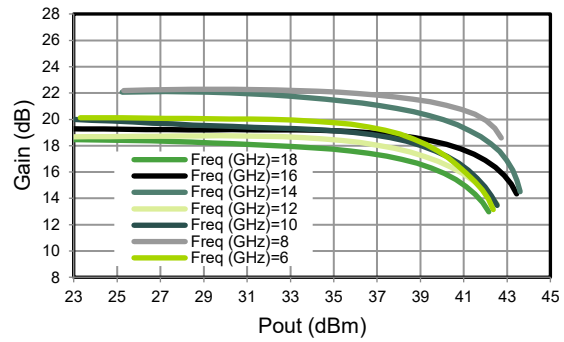


Typical Large Signal Data, CW | Test conditions unless otherwise stated V_D=24V, I_{DQ}=280mA ,TA=25 °C, CW

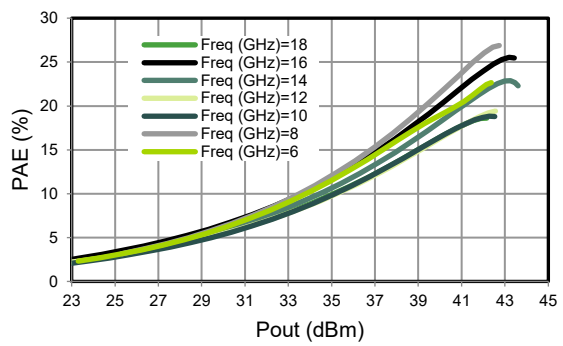
Pout vs. Pin



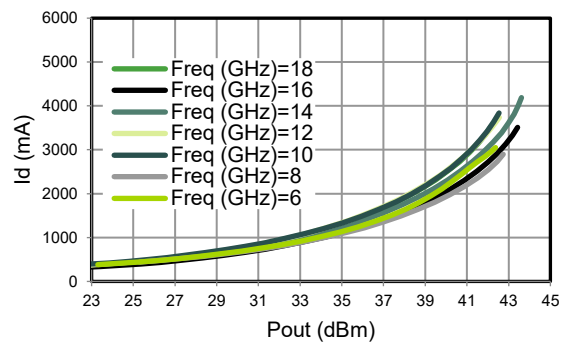
Gain vs. Pout



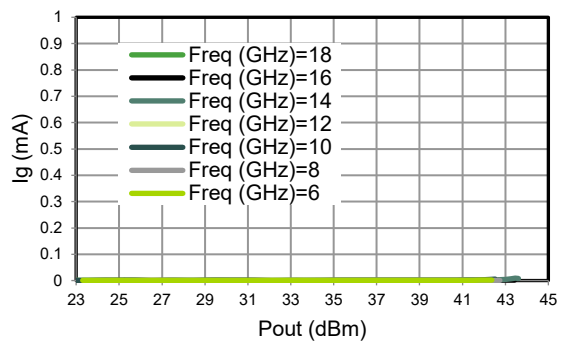
PAE vs. Pout



Id vs. Pout

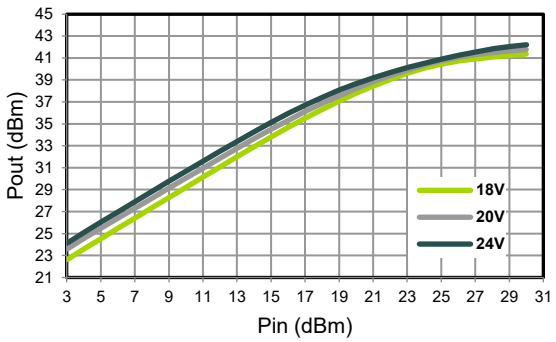


Ig vs. Pout

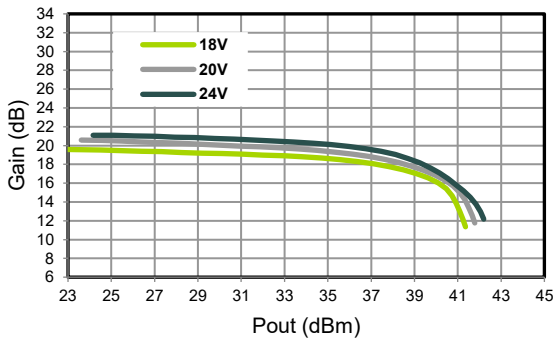


Typical Large Signal Data, CW | Test conditions unless otherwise stated V_D=18V, 20V,24V, I_{DQ}=280mA ,TA=25 °C, CW

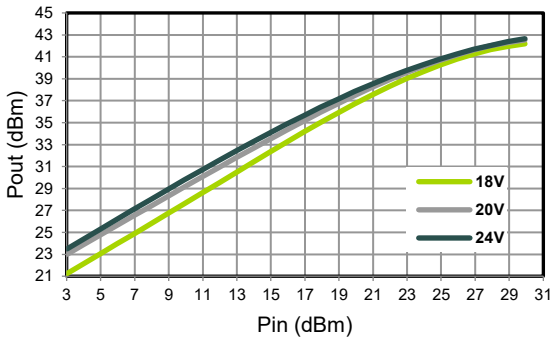
Pout vs. Pin @6GHz



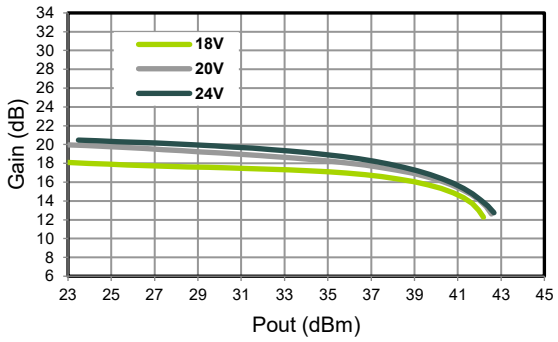
Gain vs. Pout @6GHz



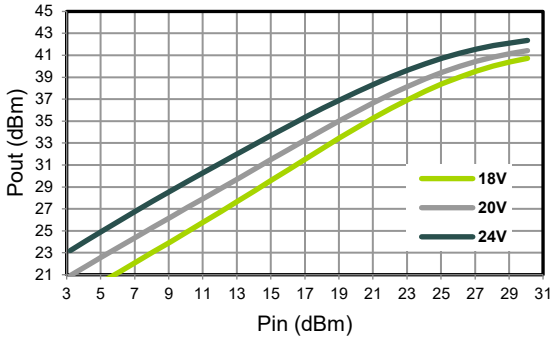
Pout vs. Pin @12GHz



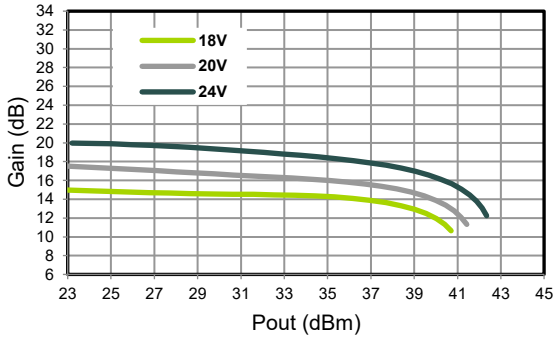
Gain vs. Pout @12GHz



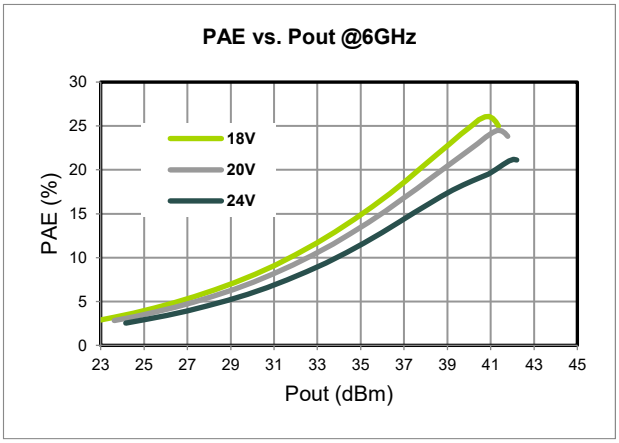
Pout vs. Pin @18GHz

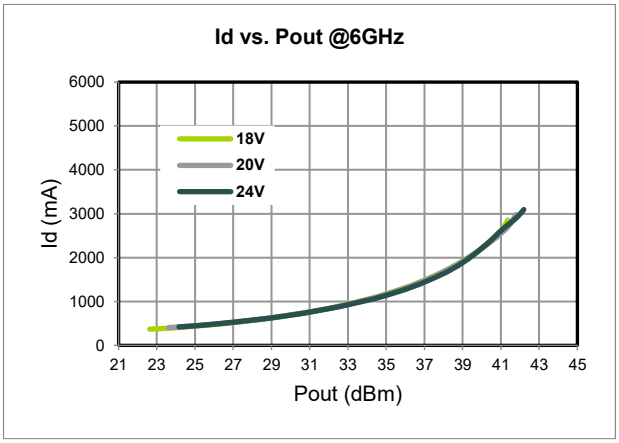


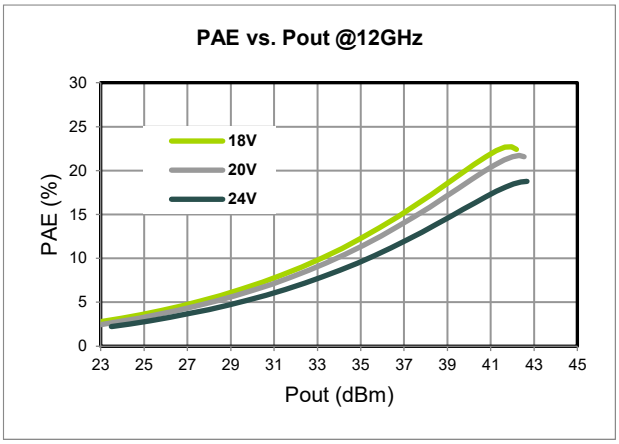
Gain vs. Pout @18GHz

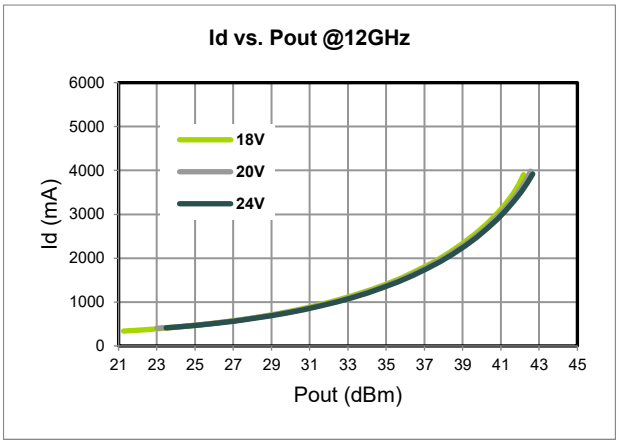


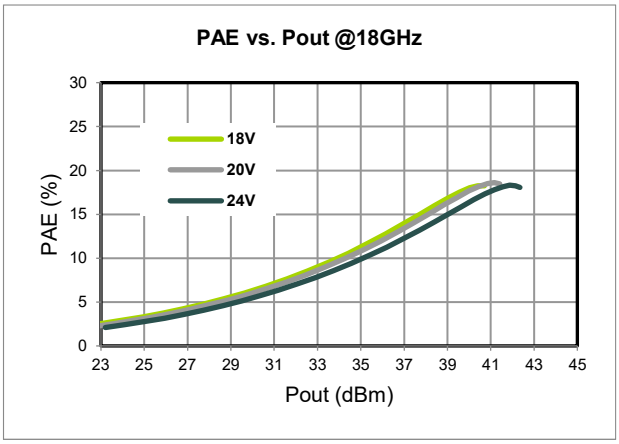
Typical Large Signal Data, CW | Test conditions unless otherwise stated V_D=18V, 20V,24V, I_{DQ}=280mA ,TA=25 °C, CW

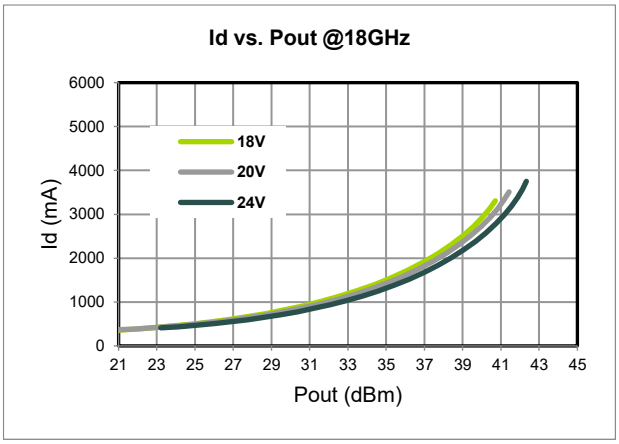




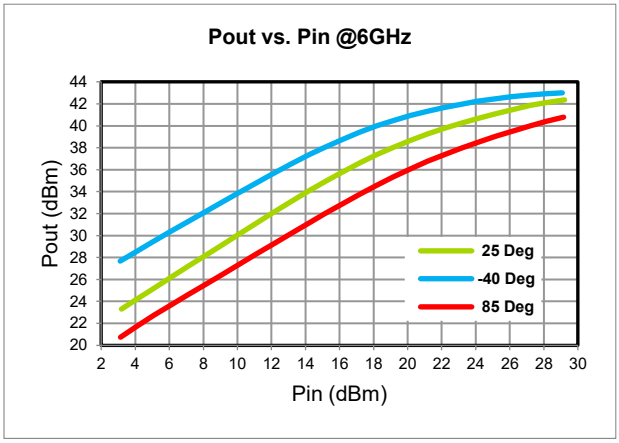


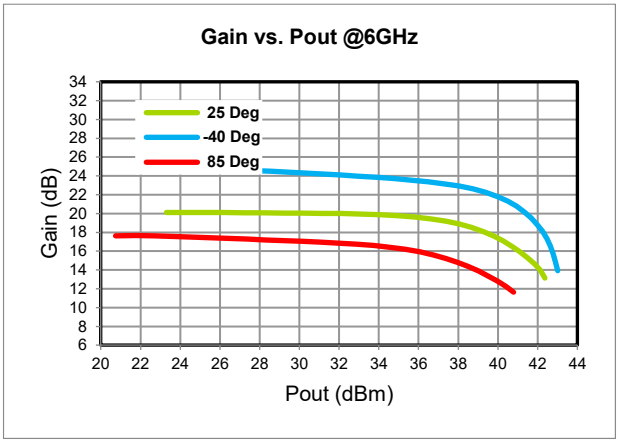


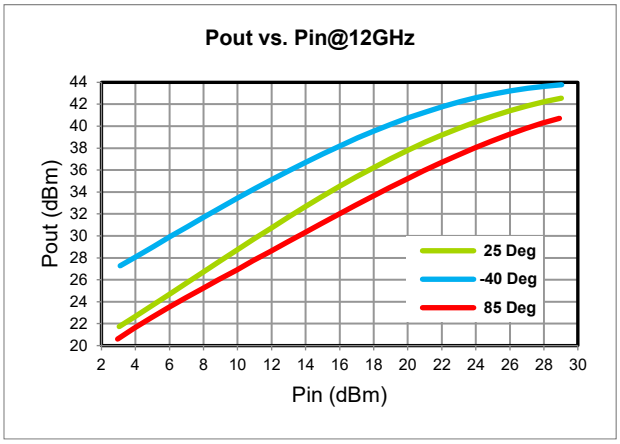


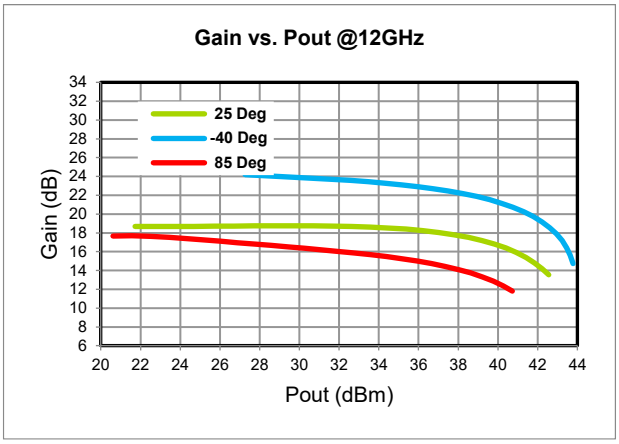


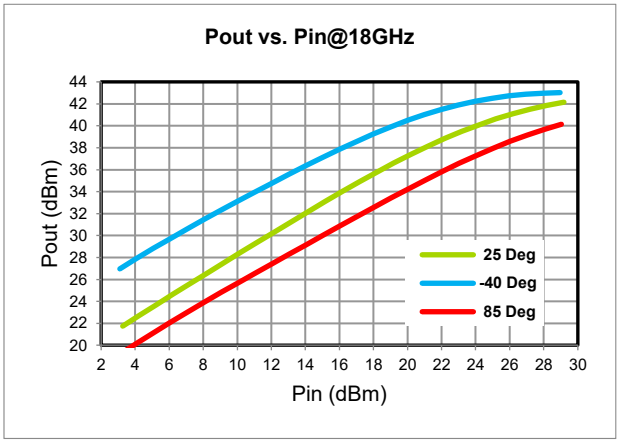
Typical Large Signal Data, CW | Test conditions unless otherwise stated V_D = 24V, I_{DQ}= 280mA , TA=25 °C, CW

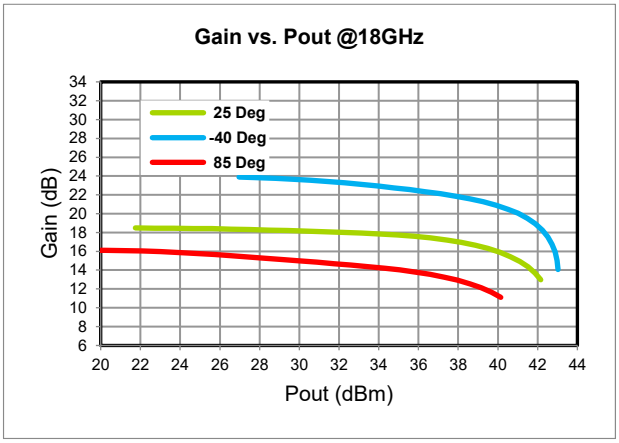




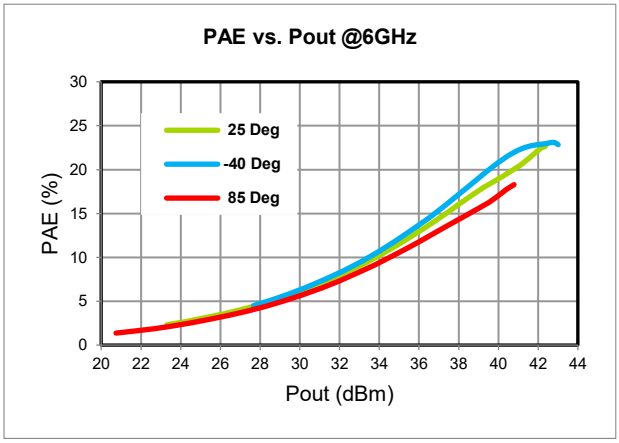


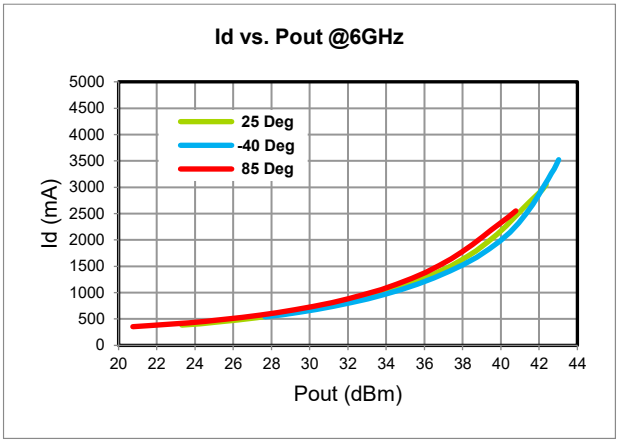


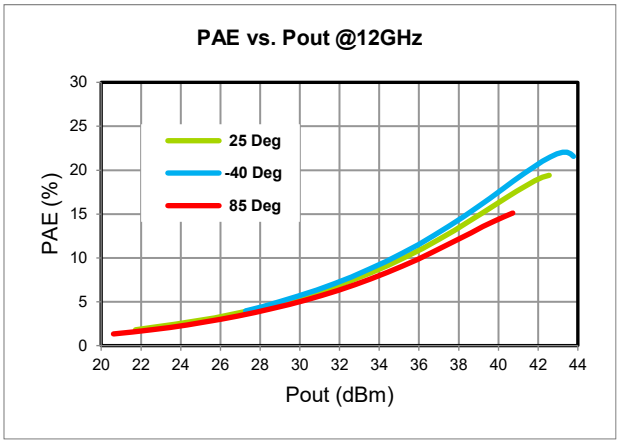


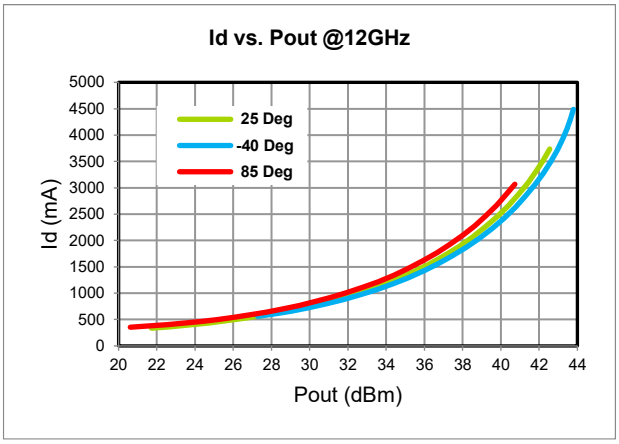


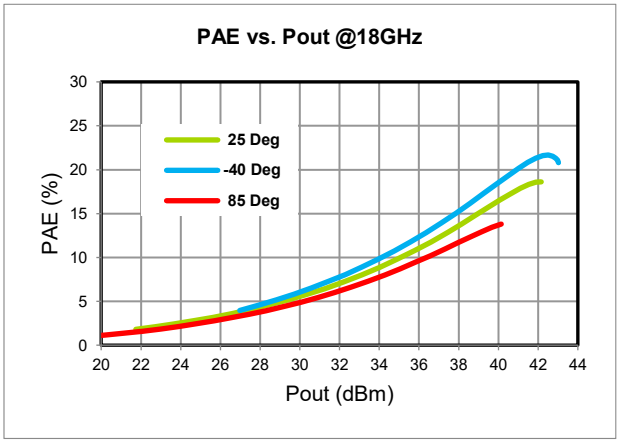
Typical Large Signal Data, CW | Test conditions unless otherwise stated V_D = 24V, I_{DQ}= 280mA , TA=25 °C, CW

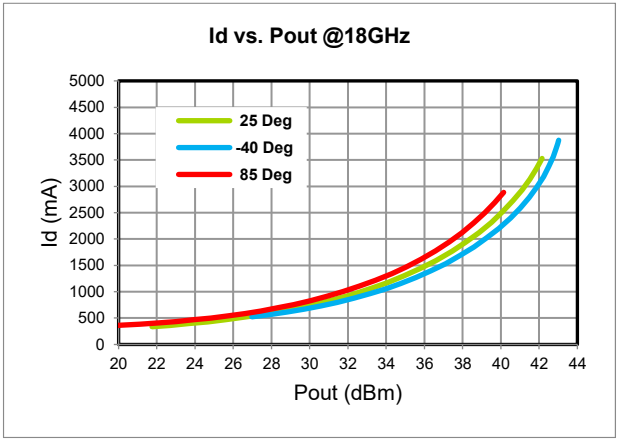




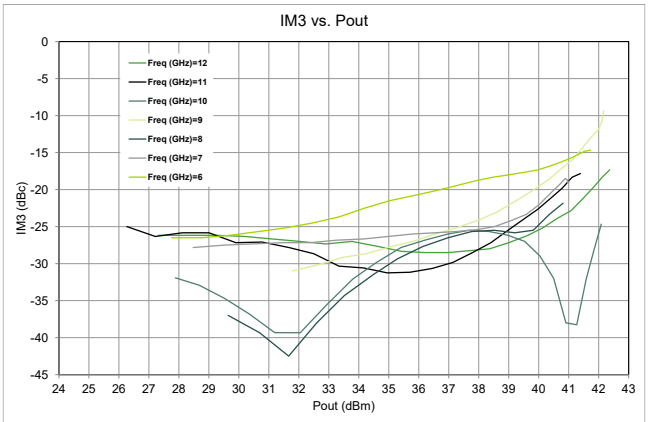


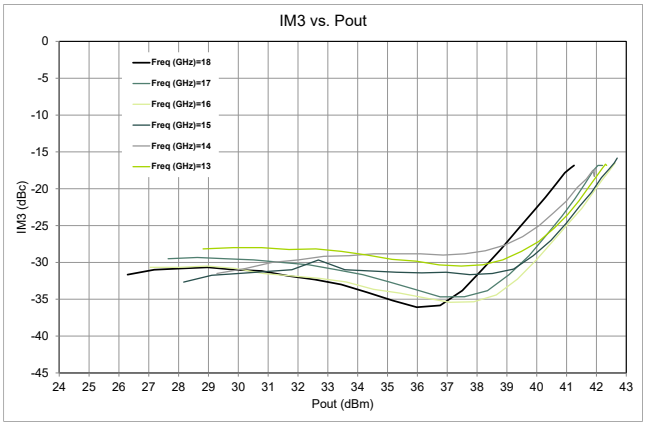




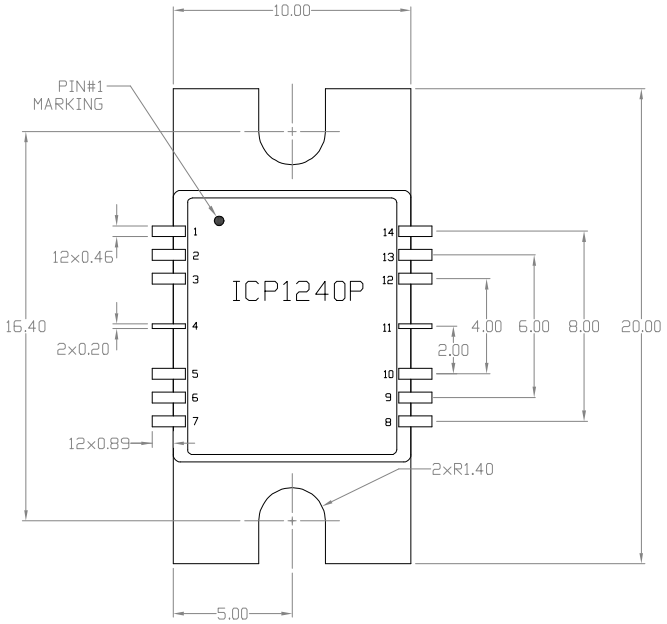


Typical Linearity Data, CW | Test conditions unless otherwise stated V_D = 24V, I_{DQ}= 280mA , TA=25 °C, Tone Spacing=10MHz CW

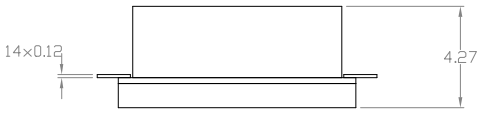




Mechanical Drawing



TOP VIEW

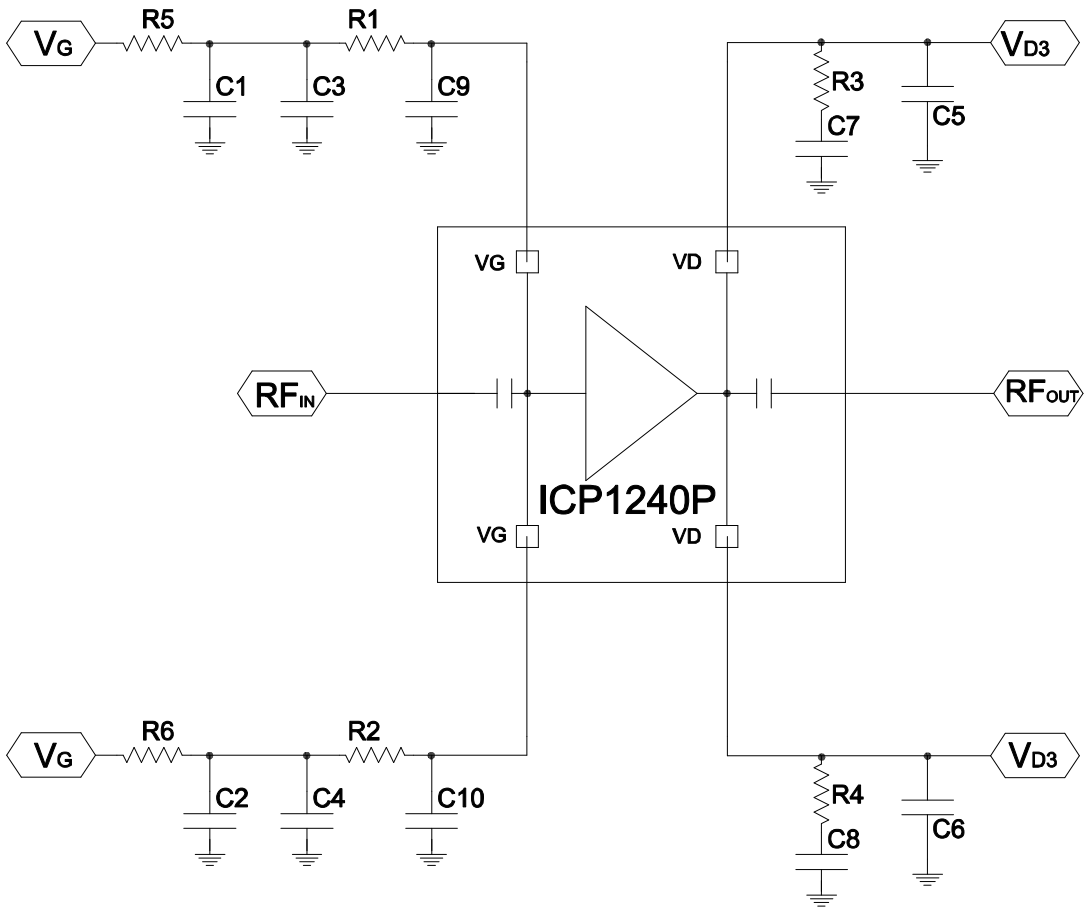


SIDE VIEW

Dimensions: mm

Pad No	Function	Description
1,7	VG	Gate bias, decoupling and bypass caps required, bias must be applied to both pins
2,6	No connect	Pin can be connected to ground or open circuit
3,5	Ground	Ground Connection
4	RFIN	50 ohm RF input, DC blocked
8,14	VD	Drain bias, decoupling and bypass caps required, bias must be applied to both pins
9,13	No connect	Second stage drain voltage, decoupling and bypass caps required, must be biased from both sides
10, 12	Ground	Ground Connection
11	RFOUT	50 ohm RF output, DC blocked
Flange	Ground	RF and DC Ground

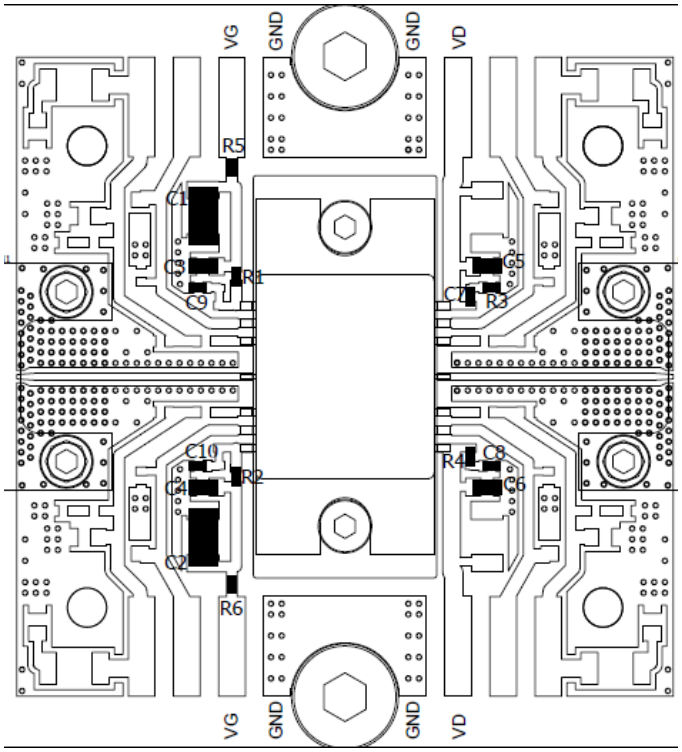
Application Circuit

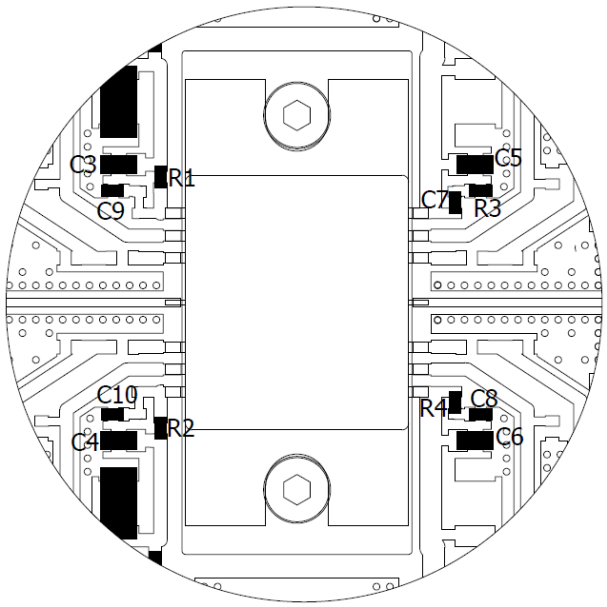


Bill of Materials

Assembly Reference	Value	Description
C1-C2	10uF	10uF Capacitor, 10%, 35V, 1206
C3 - C6	1uF	1uF Capacitor, 10%, 35V, 0603
C7-C8	10nF	10nF Capacitor, 10%,50V, 0402
C9-C10	100nF	100nF Capacitor, 10%,35V, 0402
R1-R2	5.1Ohm	5.1ohm Resistor, 0402
R3,4	0ohm	0ohm Resistor, 0402
R5,R6	56ohm	56 ohm Resistor, wire in cable

Assembly Drawing





PCB Fabrication

PCB Construction	Material	Dimensions
METAL1_TOP	Cu + ENIPIG	0.5oz Cu plated Electroless Palladium 0.3µm Electroless Nickel 3-6µm
DIELECTRIC	RO4003C	8mils (203.2µm)
METAL2_BOTTOM	Cu + ENIPIG	0.5oz Cu plated Electroless Palladium 0.3µm Electroless Nickel 3-6µm

Key Features	Dimensions
VIA Drill	0.3mm
VIA Plating Thickness	15um
50 Ohm LINE WIDTH	420um

Assembly Guidance

The package must be bolted to a thermally conductive base plate and the pins aligned with the PCB tracks. For optimum thermal transfer use an electrically conductive thermal compound before fixing the package.

Solderability

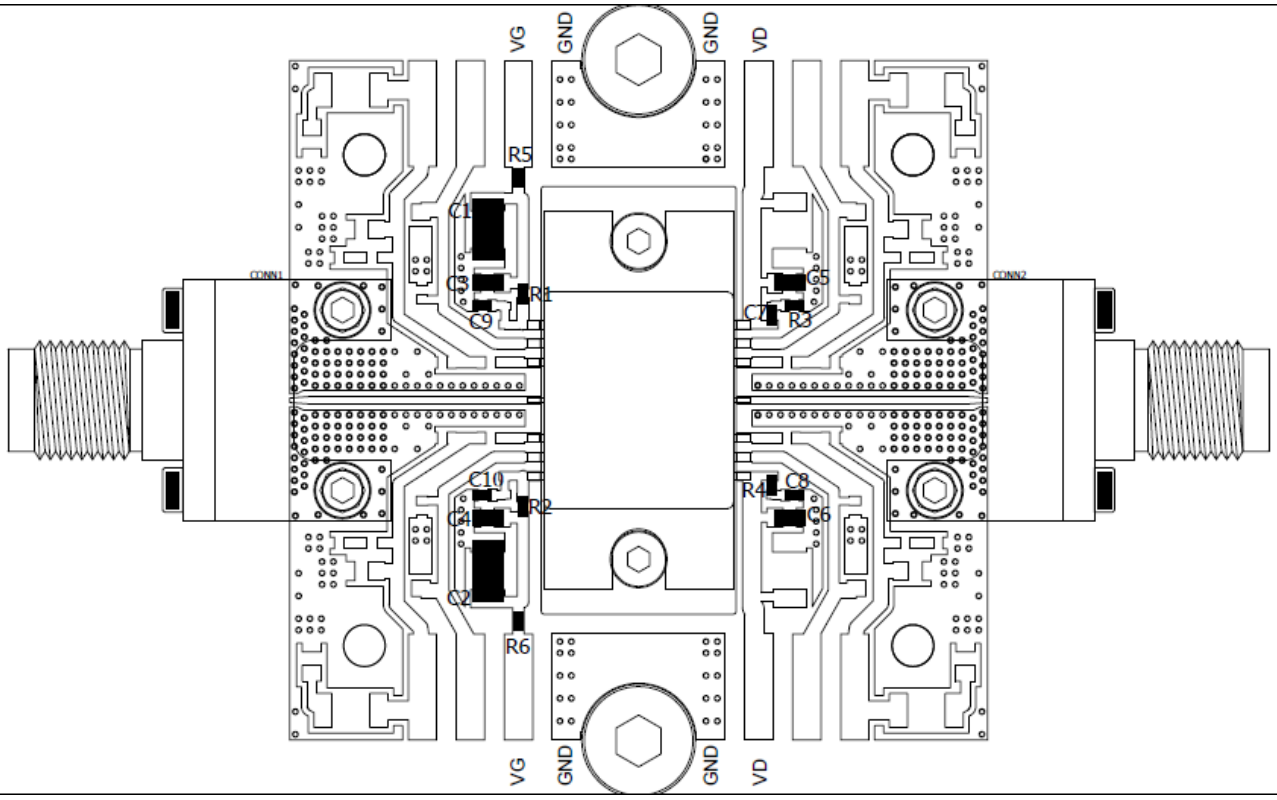
Its recommended to manually solder the leads to the PCB using a no-clean solder. This avoids washing the part after soldering.
Components are compatible lead-free solder with a temperature of 260ºC

Assembly Guidance continued.

For optimum RF and thermal performance IconicRF recommends the die assembly base plate is adequately bolted to an forced air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 170µm thick) for optimal heat transfer.

There are many variables of the second level assembly between the die base plate and heat sink that IconicRF are unable to control and the following guidance is provided as information only. Fixing bolts should be provided as close to the die as possible to ensure a optimum pressure between the base plate and the heat sink.

The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised all surfaces be cleaned and be free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star shaped pattern to a recommended torque of 2.5N/m.



Bias-Up Procedure

1. Set V_G=-5V
2. Set V_D to 20-24V
3. Adjust V_G positive until I_D quiescent is 84mA
4. Limit I_D to 1.5A
5. Apply RF Signal

Bias-down Procedure

1. Turn off RF
2. Turn off V_D, allow drain capacitor to discharge
3. Turn off V_G.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices. Class 1A HBM (250-500V) ESD Classification is anticipated.

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