

Features

- Frequency Range: 17-21GHz
- Pout: 37 dBm @ 15dBm Pin
- PAE: >30 %
- Small Signal Gain: 28dB
- Bias: VD=24V IDQ=84mA
- Technology: GaN-on-SiC
- Lead-free and RoHS compliant
- Die Size: 3.2 mm x 2.6 mm

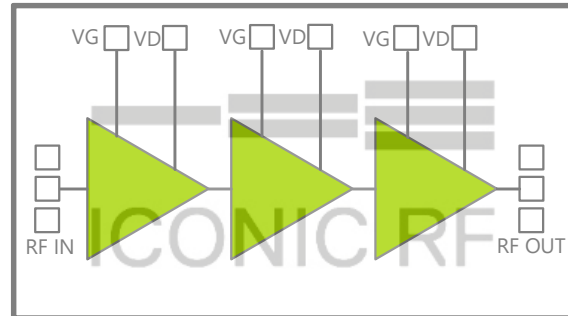
Applications

- Point-to-Point Microwave Radio
- Satellite Communications

Description

The ICP1937 is a three stage MMIC power amplifier in bare die form, fabricated using GaN-on-SiC technology. The PA operates from 17-21GHz with 37dBm output power, >30% PAE and 28dB small signal gain. The die has integrated DC blocking capacitors and is matched to 50 Ohms on the RF input and output ports. The operating frequency provides flexible operation for a variety of applications including satellite and point-to-point microwave radio. The ICP1937 is 100% DC and RF tested on-wafer to ensure compliance with electrical specifications.

Functional Diagram



Electrical Specifications | Test Conditions unless otherwise stated | $V_D=24V$, $I_D=84mA$, $T_A=25^\circ C$, CW

Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency		17.7		21.2	GHz
Output Power @ P_{sat}	Pin=15dBm		37		dBm
PAE @ P_{sat}	Pin=15dBm		30		%
Small Signal Gain			28		dB
Input Return Loss			12		dB
Output Return Loss			8		dB
I_{DQ}			84		mA
V_{GS}			1.85		V
ID drive	Pout 37dBm		900		mA

Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain Voltage (V_D)	30.0V
Gate Voltage Range (V_G)	-5 to 0V
Gate Current (I_G)	5mA
Drain Current (CW) $T_A=25^\circ\text{C}$	2.43A
Power Dissipation (CW) $T_A=25^\circ\text{C}$ Power Dissipation (CW) $T_A=85^\circ\text{C}$	58W 40W
CW Input Power 50ohm, $T_A=25^\circ\text{C}$	+20dBm
Channel Temperature	275°C
Storage Temperature	-65°C to +150°C
Input Power VSWR (2:1), $V_D=20\text{V}$, $I_{DQ}=84\text{mA}$ $V_D=24\text{V}$, $I_{DQ}=84\text{mA}$	20dBm
Eutectic Die Attach Temperature (30s)	320°C

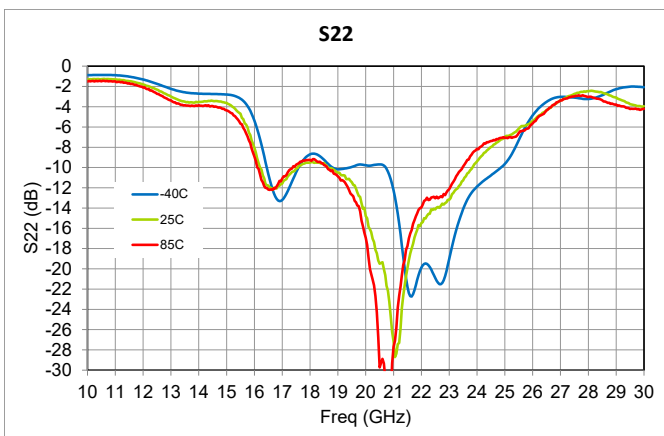
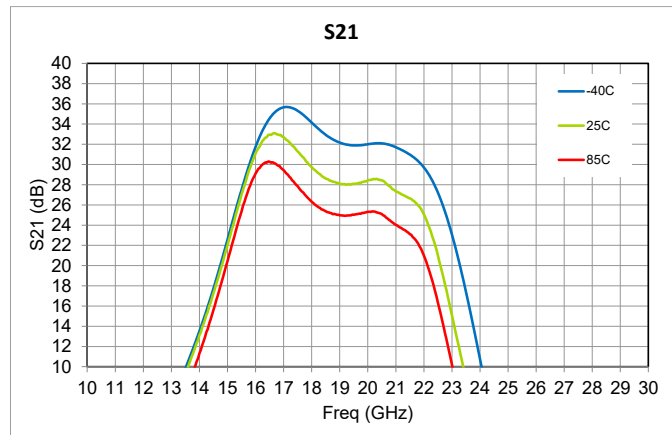
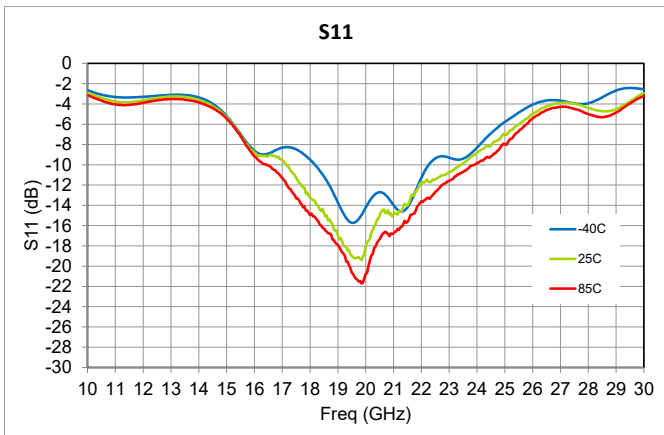
Exceeding any one or combination of these limits may cause permanent damage to this device. Microchip Technology does not recommend sustained operation near these survivability limits.

Ordering Information

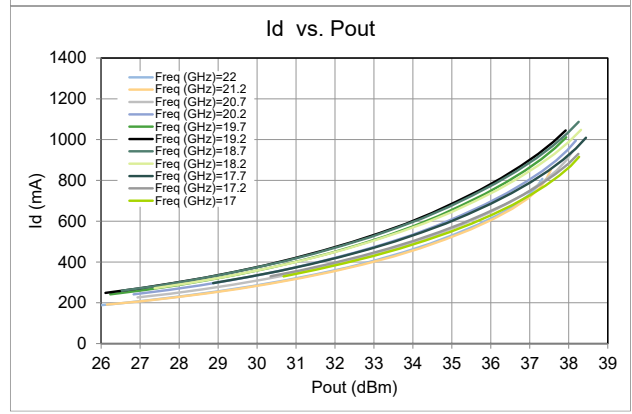
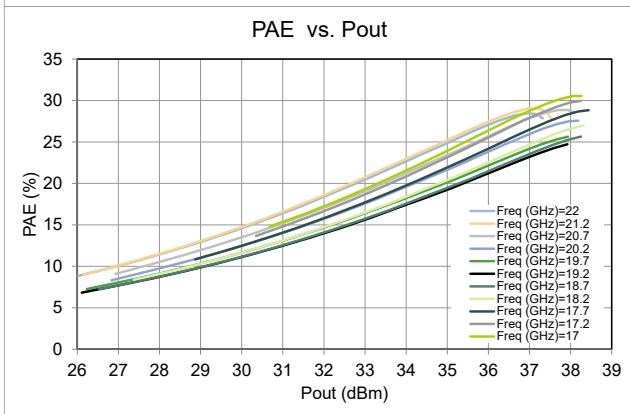
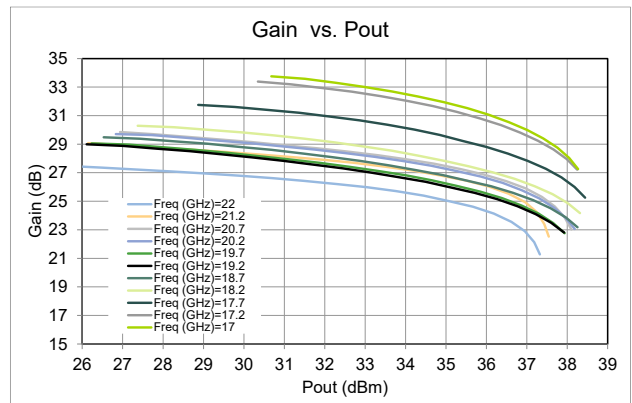
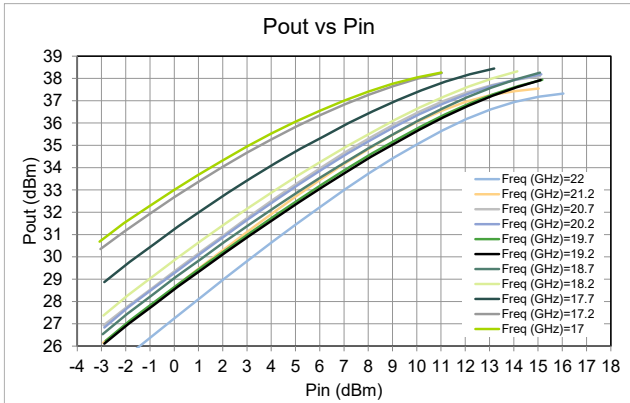
Part No.	Description
ICP1937-1-110I	Bare die
ICP1937-1-501U	Evaluation Board with SMA connectors

Typical Performance

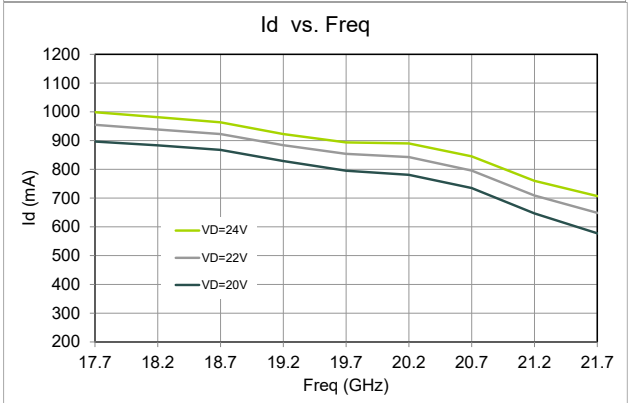
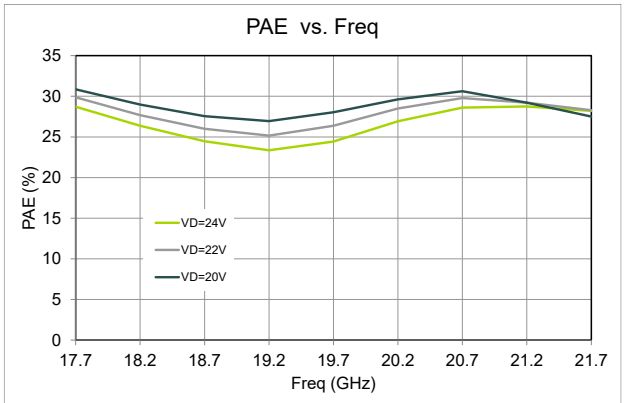
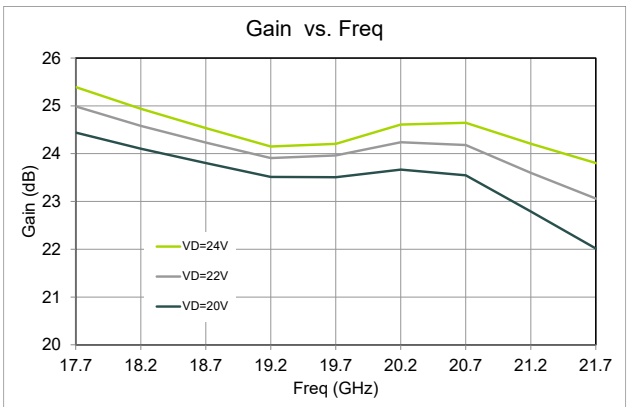
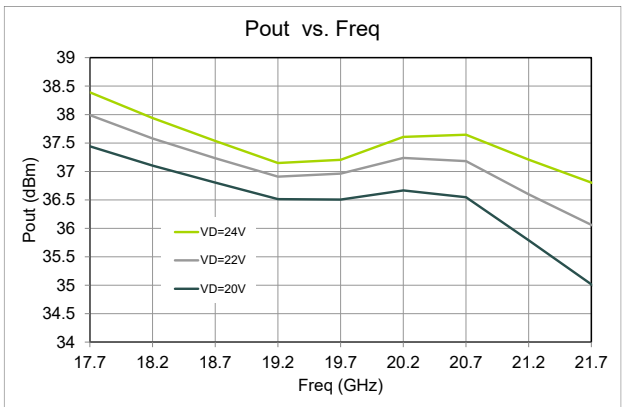
S-Parameter Performance | Test Conditions unless otherwise stated | $V_D=24\text{V}$, $T_A=-40^\circ\text{C}$, 25°C , $+85^\circ\text{C}$, $I_D=84\text{mA}$



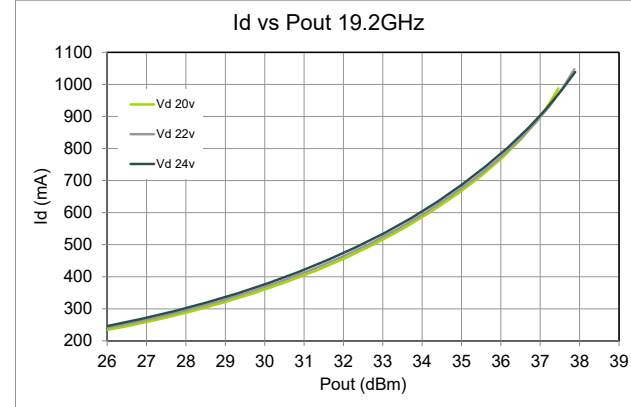
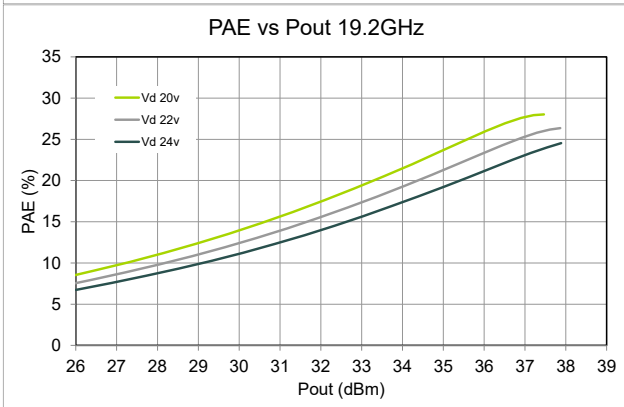
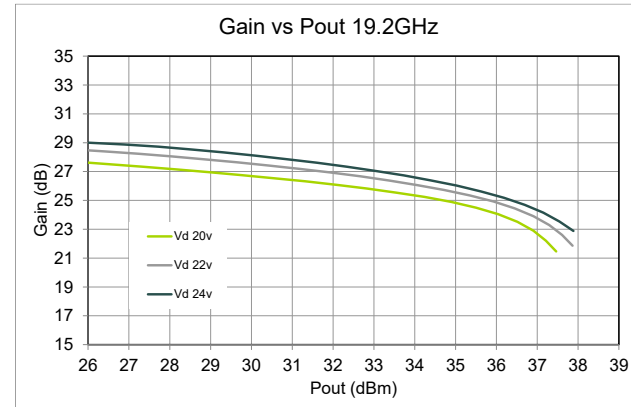
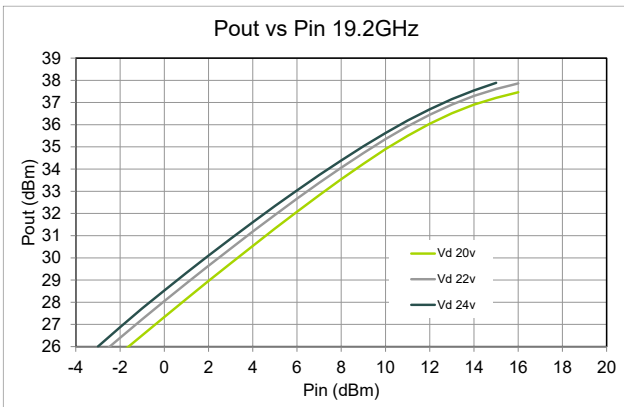
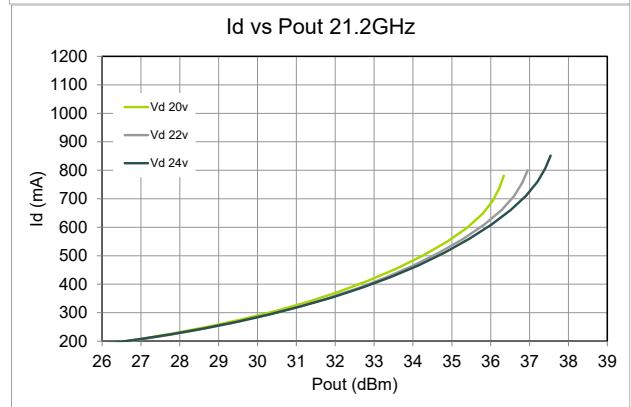
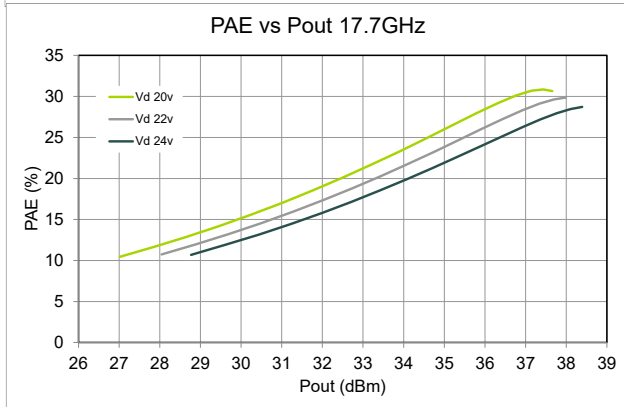
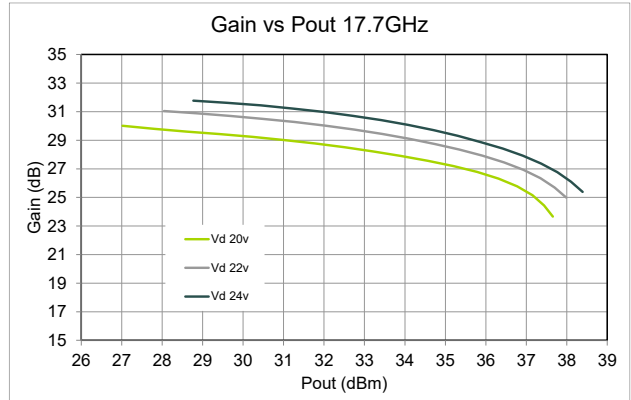
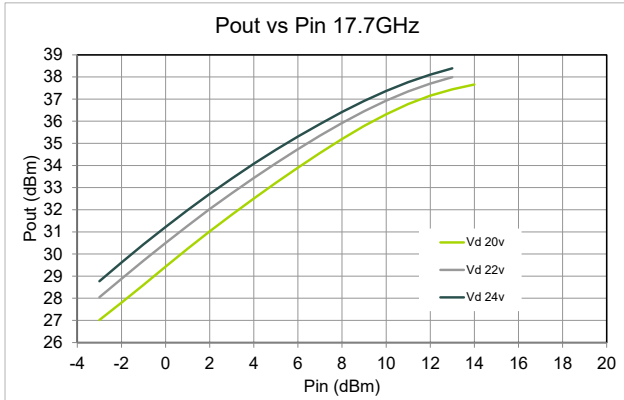
Power Performance | Test Conditions unless otherwise stated | $V_D=24V$, $I_D=84mA$, $T_A=25^\circ C$, CW



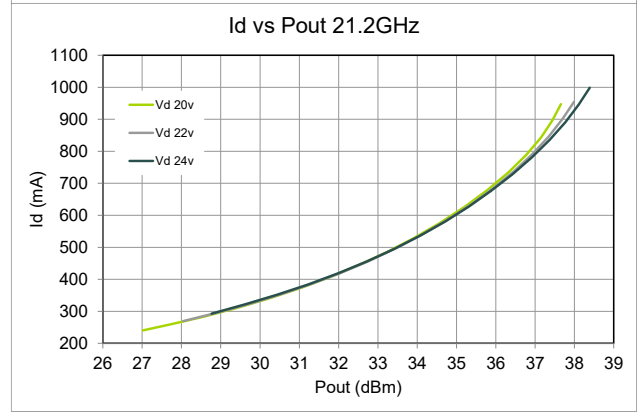
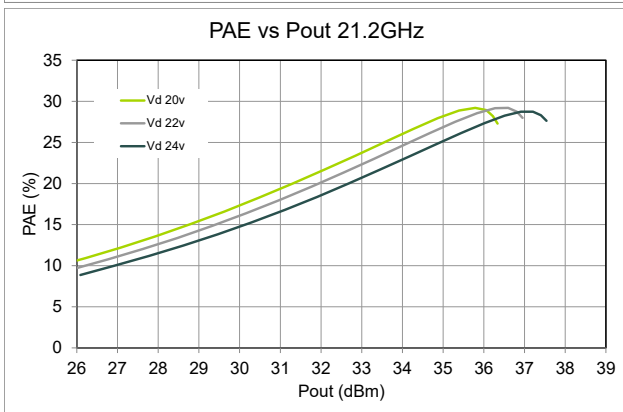
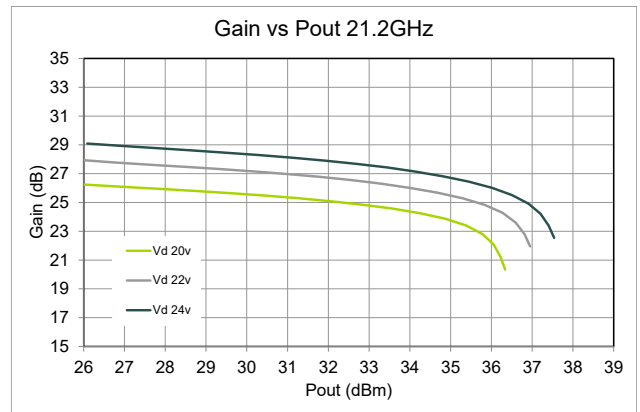
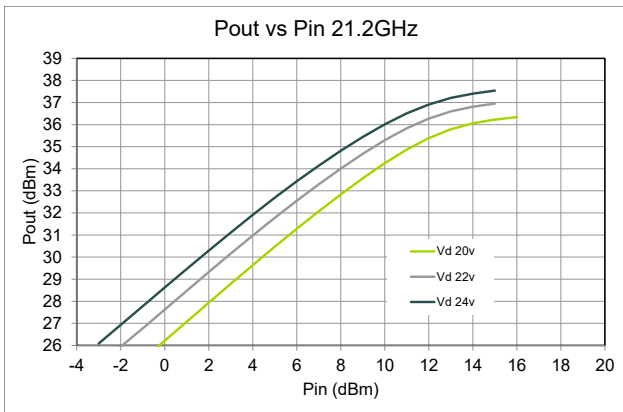
Power Performance vs Frequency | Test Conditions unless otherwise stated | $P_{in}=13dBm$, $I_D=84mA$, $T_A=25^\circ C$, CW



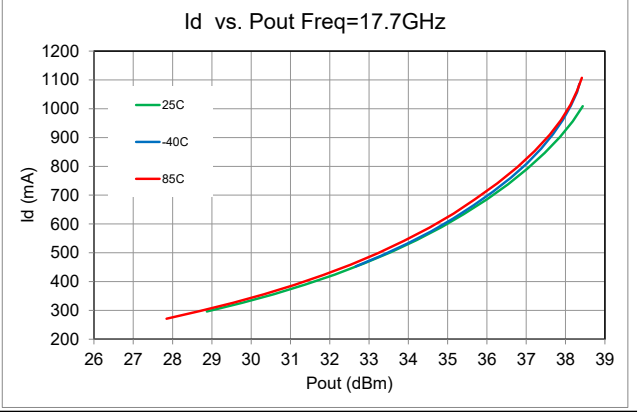
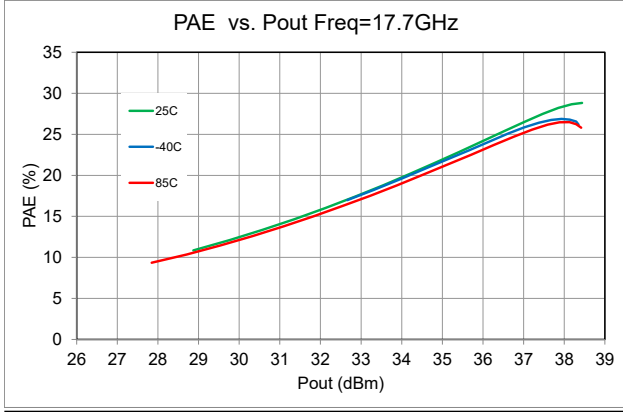
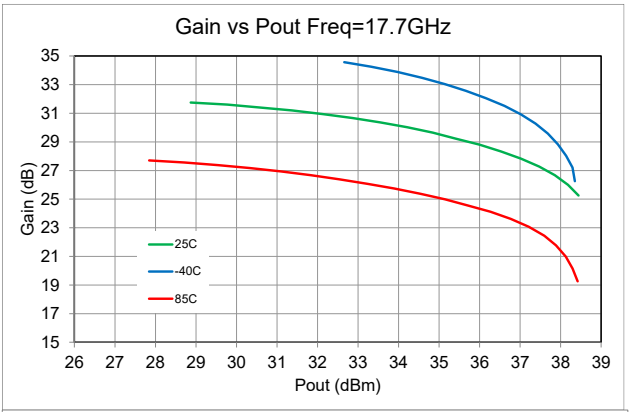
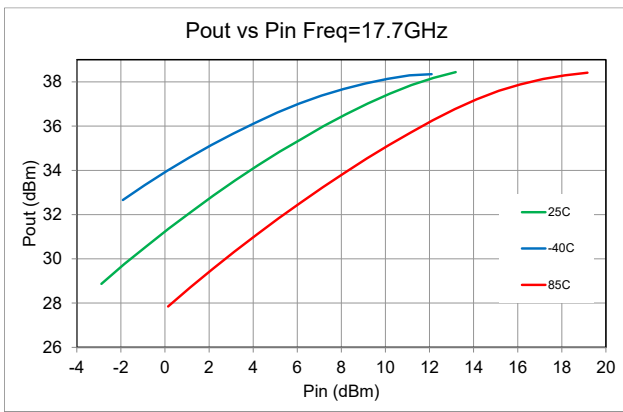
Power Performance | Test Conditions unless otherwise stated | $V_D=20V, 22V, 24V, I_D=84mA, T_A=25^\circ C, CW$



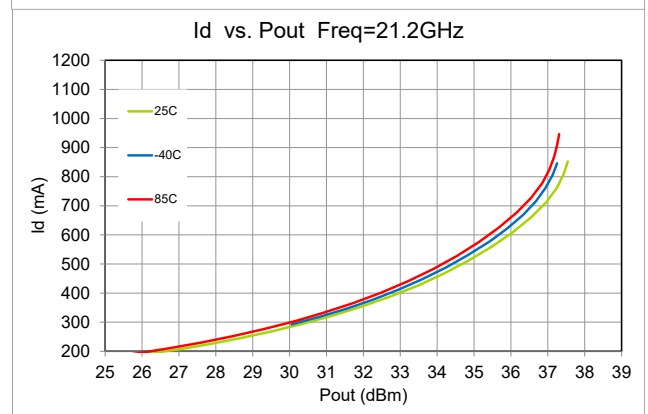
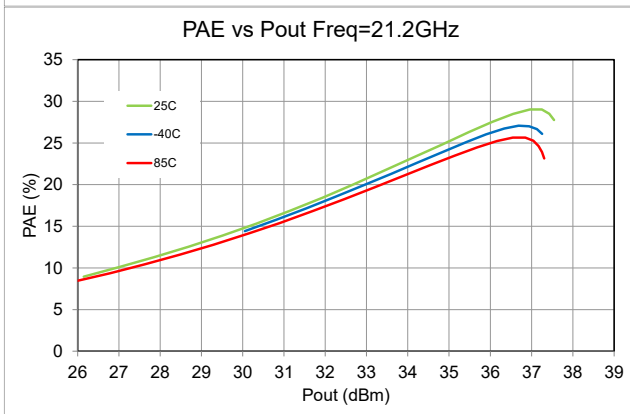
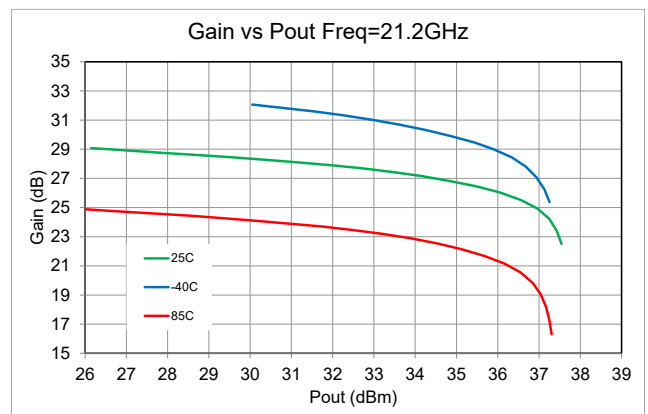
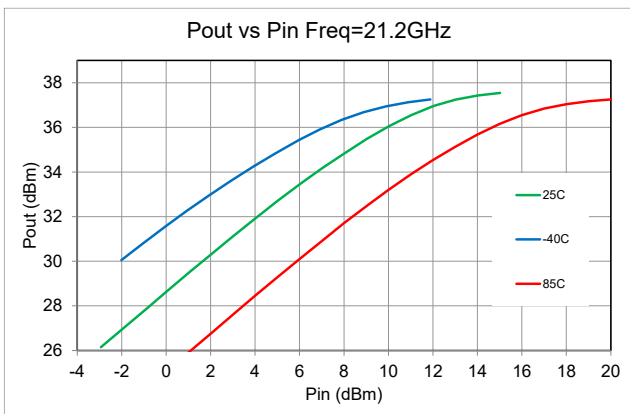
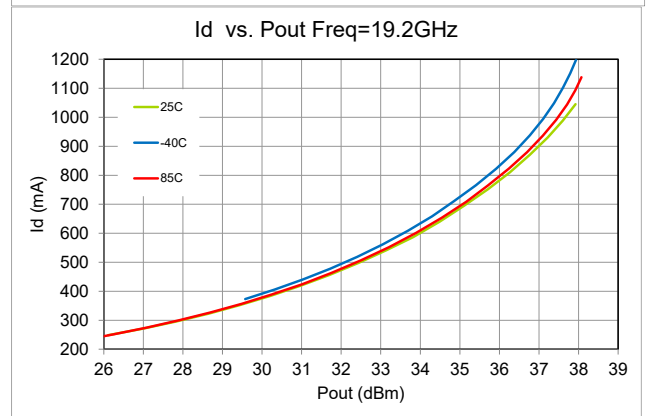
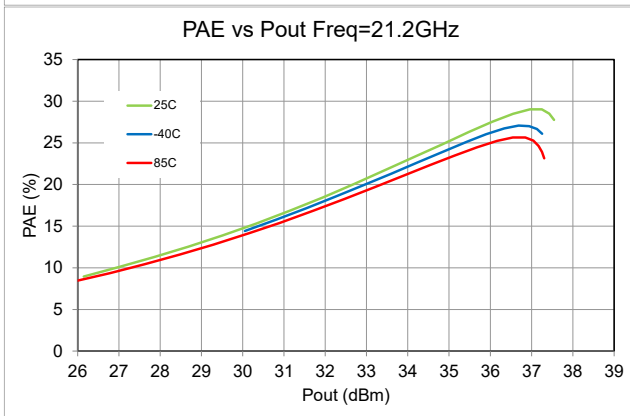
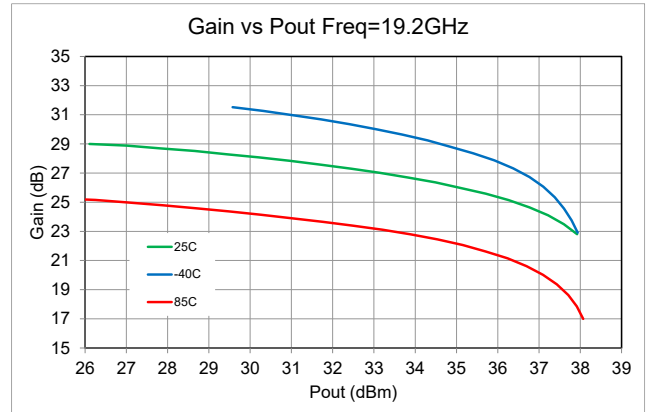
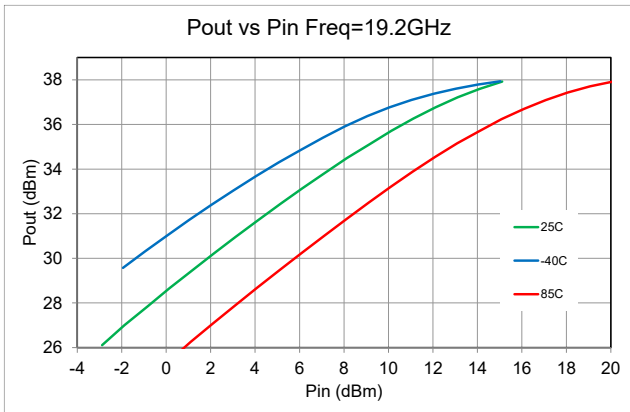
Power Performance | Test Conditions unless otherwise stated | $V_D=20V, 22V, 24V, I_D=84mA, T_A=25^\circ C, CW$



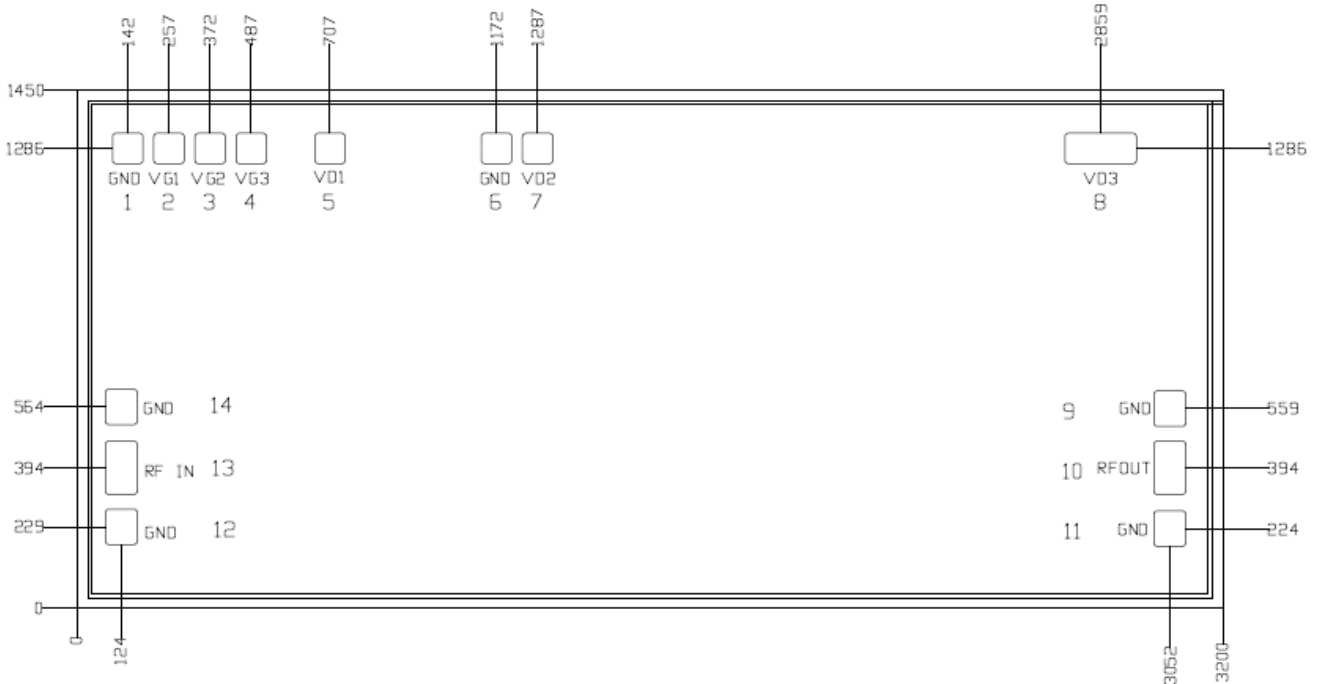
Power Performance | Test Conditions unless otherwise stated | $V_D=24V, I_D=84mA, CW, Temperature=40^\circ C, +25^\circ C, +85^\circ C$



Power Performance | Test Conditions unless otherwise stated | $V_D=24V$, $I_D=84mA$, CW Temperature= $-40^{\circ}C$, $+25^{\circ}C$, $+85^{\circ}C$



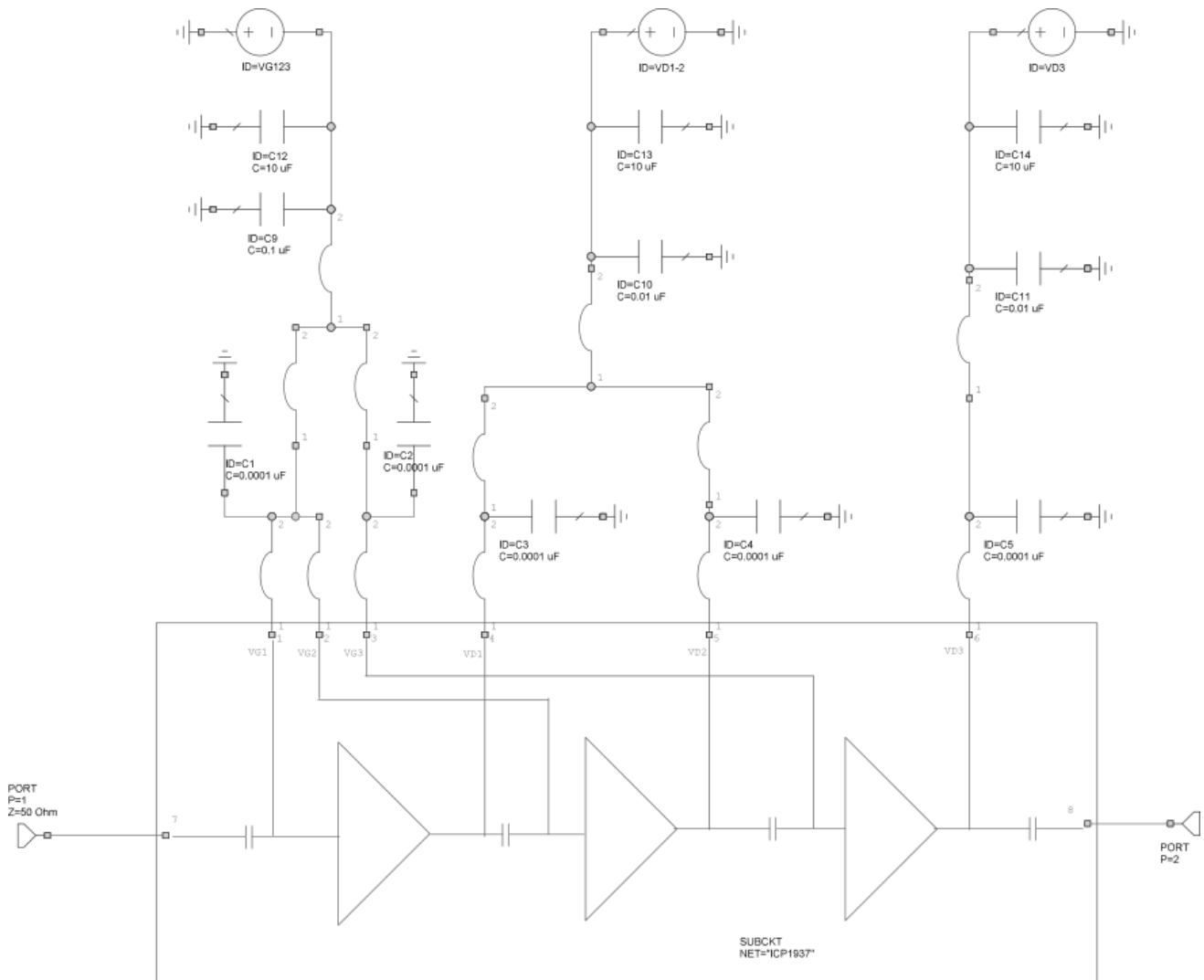
Mechanical Drawing



Units: μm
 Thickness: 100 μm
 Backside of Chip is RF and DC ground

Pad No	Pad Size (um)	Function	Description
1	89 x 150	GND	Ground
2	85 x 85	VG1	First stage gate bias, decoupling and bypass caps required
3	85 x 85	VG2	Second stage gate bias, decoupling and bypass caps required
4	85 x 85	VG3	Third stage gate bias, decoupling and bypass caps required
5	85 x 85	VD1	First stage drain voltage, decoupling and bypass caps required
6	89 x 150	GND	Ground
7	85 x 85	VD2	Second stage drain voltage, decoupling and bypass caps required
8	200 x 85	VD3	Third stage drain voltage, decoupling and bypass caps required
9,11,12,14	89 x 100	GND	Ground Pads
10	89 x 150	RF OUT	RF Output
13	89 x 150	RF IN	RF Input

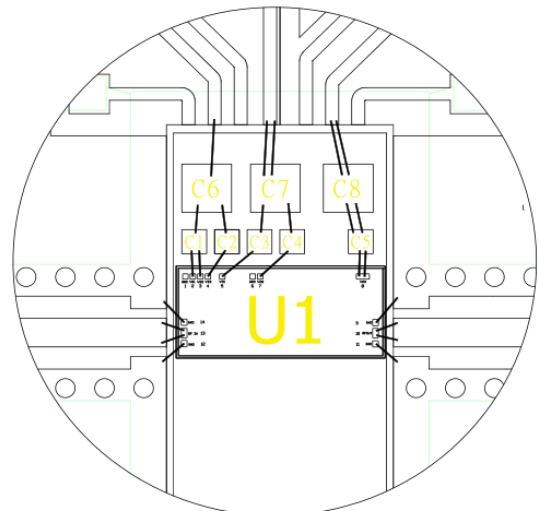
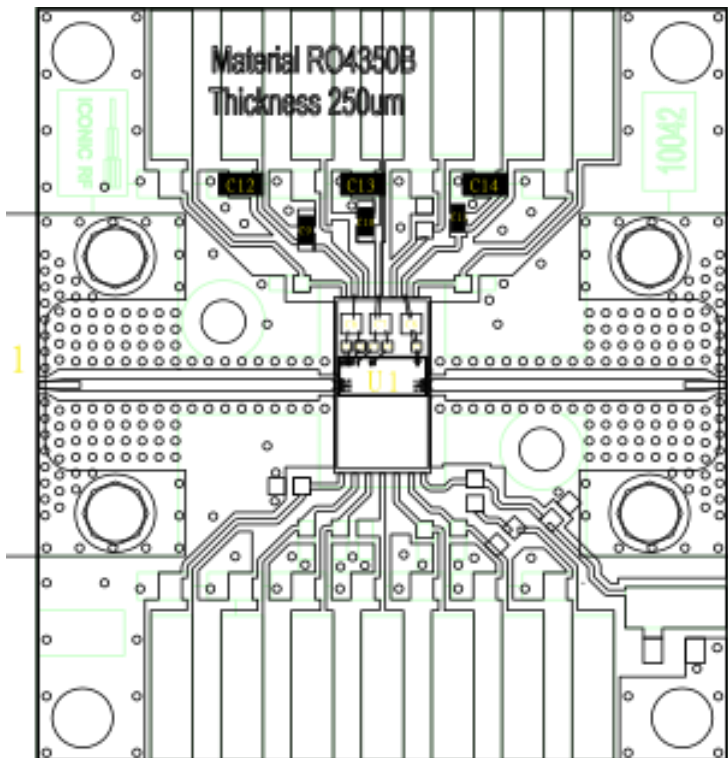
Application Circuit



Bill of Materials

Assembly Reference	Value	Description	Manufacturer Part No.
U1		ICP1937 MMIC	ICP1937
C1-C5	100pF	SLC Capacitor	Johanson 500U01A101MT4W
C6-C8	10000pF	SLC Capacitor	Knowles V30BZ103M1SX
C9	100nF	0402 size Capacitors	Various
C10,C11	10nF	0402 size Capacitors	Various
C12-C14	10uF	0603 size Capacitors	Various

Assembly Drawing



DETAIL A - BONDING
SCALE 5 : 1

Assembly Guidance

Optimum RF power performance is achieved by minimizing output RF bond wire length.

Interconnect assembly Notes

- Ball Bonding is preferred technique
- Force, time and ultrasonic parameters are critical.
- Aluminum wire bonding is not recommended.
- Bond Wire diameter of 1mil is recommended.

Die attach of component using adhesive

- Vacuum collets are preferred method of pickup.
- Pickup method must consider the avoidance of die air bridges.
- Die suitable for Eutectic and Epoxy die attach.

- Where Epoxy is used, high thermal conductivity Silver Sintered Epoxy is recommended:-
 - Namics H9889-1

Reflow Process

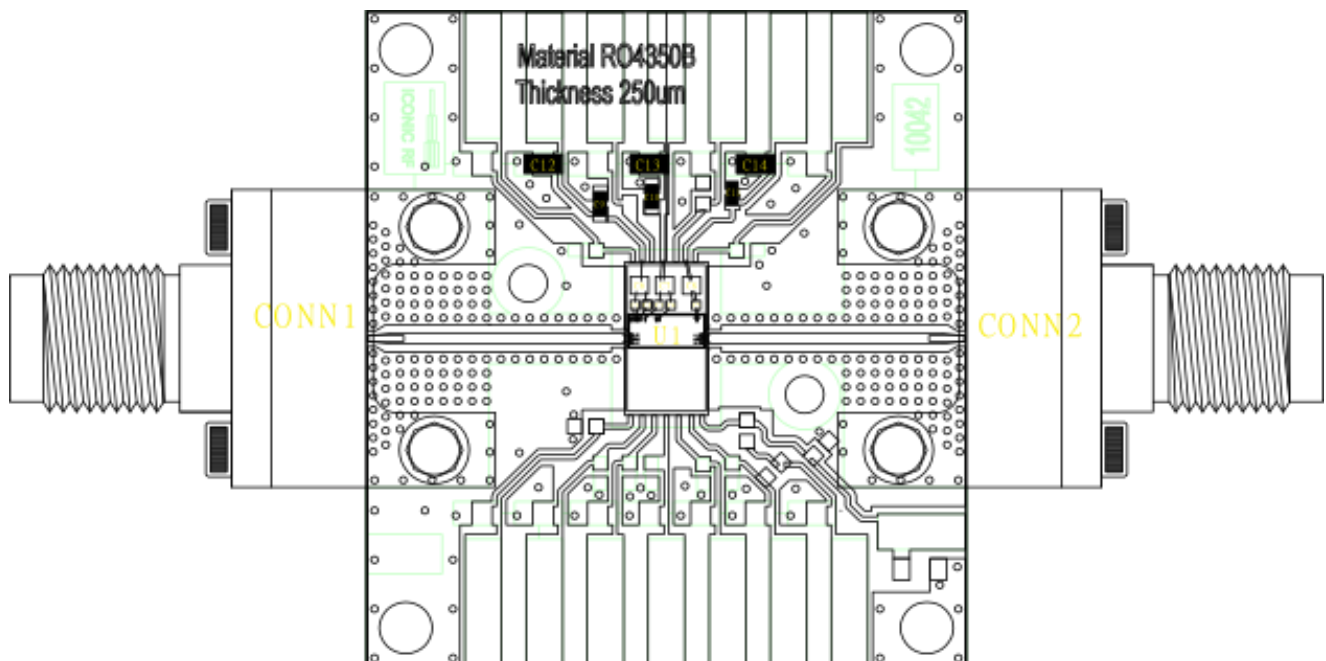
- Maximum temperature 320°C for 30 seconds.
- Material matching for coefficient of thermal expansion is crucial for long-term reliability

Assembly Guidance continued:

For optimum RF and thermal performance Microchip Technology recommends the die assembly base plate is adequately bolted to an forced air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 170 μ m thick) for optimal heat transfer.

There are many variables of the second level assembly between the die base plate and heat sink that Microchip Technology is unable to control, and the following guidance is provided for information only. Fixing bolts should be provided as close to the die as possible to ensure an optimum pressure between the base plate and the heat sink.

The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised all surfaces be cleaned and be free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star shaped pattern to a recommended torque of 2.5 N/m.



Bias-Up Procedure

1. Set $V_G = -5V$
2. Set V_D to 20-24V
3. Adjust V_G positive until I_D quiescent is 84mA
4. Limit I_D to 1.5A
5. Apply RF Signal

Bias-down Procedure

1. Turn off RF
2. Turn off V_D , allow drain capacitor to discharge
3. Turn off V_G .

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices. Class 1A HBM (250-500V) ESD Classification is anticipated.

